Control Strategies, Robustness Analysis, Digital Simulation and Practical Implementation for a Hybrid APF with a Resonant Ac-link

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Abstract: This paper proposes a novel hybrid active power filter (HAPF) topology based on the cascaded connection of the AC-side capacitor and the third-order LCL-filter, which has the advantage of the conventional hybrid filter and the LCL-filter in terms of reduced dc-link voltage and better switching ripple attenuation. The robust deadbeat control law is derived for the current loop, with special emphasis on robustness analysis. The stability and robustness analysis under parameter variations are presented for the converter-side current tracking scheme and the grid-side current tracking scheme. It is found that the stability margins obtained from the converter-side current tracking control scheme are generally higher than those obtained from the grid-side current tracking scheme. However, the converter-side current tracking scheme is sensitive to the variation of the damping resistance, and it would impose additional parameter uncertainty on the control system and complicate the problem. Hence the grid-side current tracking scheme is implemented. The simulation results obtained from Matlab/Simulink are presented for verification, where the inductance variation and grid disturbance scenarios are also taken into consideration. The effectiveness of the proposed hybrid APF is substantially confirmed by the simulation and experimental results.

Keywords: power quality; harmonic estimation; active filter; hybrid; robustness analysis; digital signal processor (DSP)

1 Introduction

Due to the proliferation of nonlinear loads in electric power distribution systems, electrical power quality has been an important and growing problem Particularly, power quality problems are causing detrimental effects for customers; these problems result from current harmonics produced by nonlinear loads, e.g., variable ac motor drives, HVDC systems, arc furnaces, grid-connected renewable energy resources and household appliances. The increased harmonic pollution causes a significant increase in line losses, instability, and voltage distortion when the harmonic currents travel upstream and produce voltage drop across the line impedance [1-3]. This fact has led to the proposal of more stringent requirements regarding power quality, like those specifically collected in the standards IEC-61000-3-{2,4} and IEEE-519 [4, 5]. For several decades, active power filters (APFs) have been recognized as the most effective solutions for harmonic compensation. Their objective is to suppress the current harmonics and to correct power factor (PF), especially in fast-fluctuating loads [2]. A lot of recent literature has tried to improve APFs by developing new topologies or new control laws [3, 6-8]. In order to provide a systematic elaboration of the recent development in APFs, a survey of the state-of-the-art techniques for the APFs is outlined herein.

It was reported in Refs. [9-13] that the performance of APF is dependent on how the reference compensating signals are generated. The instantaneous reactive power theory [9], the modified *p-q* theory [10], the synchronous reference frame (SRF) theory [11], the instantaneous i_d-i_q theory [12], and the method for the estimation of current reference by maintaining the voltage of *dc*-link [13] are reported for generating references through the subtraction of positive sequence fundamental component from the nonlinear load current. These control schemes look very attractive for their simplicity and ease of implementation, but fail to provide an adequate solution under extreme conditions of harmonics, reactive power and their combinations, with limited power rating of voltage source inverter (VSI) [14]. In such cases, to safeguard the hardware, the protection scheme isolates the APF, which leaves the system to the mercy of unwanted disturbances; or, if reference signals are saturated, then the APF becomes a source of disturbance itself. In [15], the reference generation method based on the Goertzel algorithm was proposed; however, some practical issues, i.e, the stability of the closed-loop current control algorithm and voltage regulation, have not been discussed. Other solutions to harmonic detection and reference signal generation are based on artificial intelligence (AI), particularly on neural networks (NNs) [16]. In recent literature, a slightly different approach was proposed in [17], where an adaptive linear neural network (ADALINE), trained by a least-squares algorithm (LS) [18], was used to estimate the active component of the fundamental load current. In [19], a single-phase distributed generation (DG) unit with APF capability via adaptive neural filtering (ANF) was introduced, and which does not need *a priori* training of the neural network. Hence it is neither

cumbersome nor computationally demanding, especially if compared with other neural-based techniques that require offline training [16].

Apart from the neural network approach, the genetic algorithm (GA) was also introduced for APF applications [20]. These control strategies have a common drawback concerning the global stability of the closed-loop system, which hampers its application for practical APF systems. To overcome the stability issues, the sliding-mode control (SMC) was presented in [21]. However, the calculation technique for the reference current using SMC scheme is complicated and would require more advanced and sophisticated hardware for the practical implementation of the algorithm. The direct power control (DPC), on the other hand, is an indirect current control method that originates from the instantaneous reactive power theory (IRPT) [22]. However, the main drawback of DPC is the high gain of the controller and, as a consequence, the values of the input inductors have to be very large to attenuate the current ripple, which increases the cost, size, and weight of the system [22, 23]. Recent works have introduced predictive control and model-based strategies for DPC with improved steady state and dynamic response [23], where the control loops is designed with a high gain at the selected harmonic frequencies. In [24], repetitive control was utilized for harmonic compensation, which achieves low total harmonic distortion current waveforms, but at the expense of fast sampling capabilities of the hardware. As an alternative approach, resonant harmonic compensators were presented in [25], which were based on generalized integrators connected in parallel with a conventional tracking regulator. Moreover, deadbeat current control schemes were reported in [26]; these offer the potential for achieving the fastest transient response, more precise current control, zero steady-state error, and full compatibility with digital control platforms. However, there are two main practical issues related to the deadbeat control, namely: 1) bandwidth limitation due to the inherent plant delay and 2) sensitivity to plant uncertainties.

In addition to the reference current generation schemes and the current control algorithms, the switching ripple attenuation and the electromagnetic interference (EMI) reduction are also of vital importance for the practical implementation of APFs. To resolve the issues of switching ripple and EMI reduction, normally a large value inductance for output filtering should be adopted [27]. However, a high value inductance degrades system dynamic response and also requires a higher voltage on the dc-link of the inverter, thus resulting in higher power losses. By connecting a small-rated active filter directly to the single-tuned *LC*-filter to form the hybrid topology, the dc-link voltage of the VSI can be reduced to a fraction of the mains voltages. In [27], an alternative solution for switching frequency reduction using *LCL*-filter-based topology was presented.

In order to take the advantage of the hybrid *LC*-filter topology for reduced dc-link voltage and the *LCL*-filter for better switching ripple attenuation, a novel hybrid APF (HAPF) configuration is proposed in this paper. It resembles the single-tuned *LC*-filter-based hybrid topology at lower frequency range, and thus the dc-link

voltage of the VSI is remarkably reduced. By using a third-order *LCL*-filter to replace the *L*-section of the resonant *LC*-filter, the total filter inductors are significantly reduced and satisfactory switching ripple attenuation is achieved. The adaptive linear neural network [28] is utilized for harmonic estimation and reference current generation for the proposed hybrid APF. Additionally, the deadbeat control law [26] is derived based on the low frequency equivalent model of the *LCL*-filter section of the inverter power-stage. A novel average current tracking scheme is proposed to enhance the performance of the deadbeat control algorithm. The selective harmonic compensation is achieved by using the ADALINE-based harmonic estimation scheme, which significantly reduces controller bandwidth and thus enhances system stability. To validate the proposed APF and its control strategies, extensive simulation results are presented. And a prototype system is also built. The laboratory experiments are also provided, and these are consistent with the theoretical analysis and simulation results.

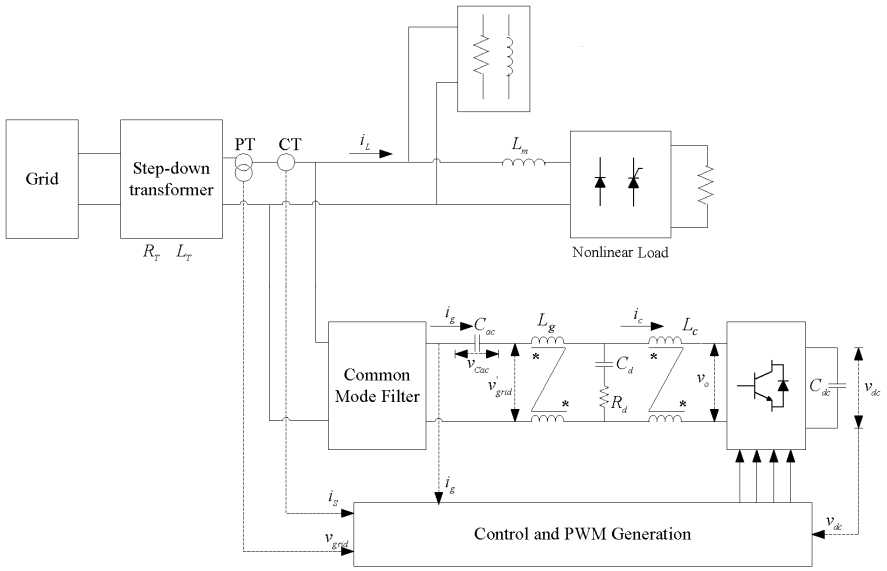


Figure 1
Single-phase schematic of the proposed hybrid active power filter

The organization of this paper is as follows. The mathematical formulation of the proposed HAPF is presented in Section 2. Three aspects related to the control system are discussed in Section 3, namely, the ADALINE-based harmonic estimation scheme, the feedback plus feed-forward control scheme and the dc-link voltage regulation of the VSI. The simulation results and experimental results are presented in Sections 4 and 5, respectively. Finally, Section 6 concludes this paper.

2 Mathematical Model of the Proposed Hybrid APF

Fig. 1 shows the circuit diagram of the proposed *LCL*-filter-based hybrid APF (HAPF). Three single-phase topologies are utilized in the laboratory prototype system as demonstrated by the experimental results; thus only the single-phase representation is illustrated herein. The *LCL*-filter, consisting of L_g, C_d and L_c with possible passive damping resistance R_d, is used as the output filter of the VSI and grid interface. The *LCL*-section is equivalent to an inductor (*L*-filter) at lower frequencies. Hence the *LC* resonant topology is formed between the *LCL*-filter and AC-side capacitor C_{ac} in the low frequency range, and thus the dc-side voltage of the VSI is remarkably reduced to achieve lower EMI emission and higher inverter efficiency. Referring to Fig. 1, the system equations can be derived according to Kirchhoff's laws, which yield:

$$\begin{cases} L_g \dfrac{di_g}{dt} + L_c \dfrac{di_c}{dt} + v_{Cac} = v_{grid} - v_o \\ i_g = C_{ac} \dfrac{dv_{Cac}}{dt} \\ i_d = C_d \dfrac{dv_{cd}}{dt} = i_g - i_c \\ v_{cd} + R_d (i_g - i_c) = L_c \dfrac{di_c}{dt} + v_o \end{cases} \tag{1}$$

where parameters i_g and i_c are inverter currents across the inductors L_g and L_c respectively, i_d and v_{cd} represent the current and voltage across the capacitor of the *RC*-filter brunch, and v_{Cac} is the voltage of the AC-side capacitor C_{ac}. Rearranging Eq. (1), the following equations can be derived:

$$\begin{cases} L_g \dfrac{di_g}{dt} = -R_d (i_g - i_c) - v_{cd} - v_{Cac} + v_{grid} \\ L_c \dfrac{di_c}{dt} = R_d (i_g - i_c) + v_{cd} - v_o \\ C_{ac} \dfrac{dv_{Cac}}{dt} = i_g \\ C_d \dfrac{dv_{Cd}}{dt} = i_g - i_c \end{cases} \tag{2}$$

Assuming $L_g = L_{0g} + \Delta L_g$, $L_c = L_{0c} + \Delta L_c$, $C_{ac} = C_{0ac} + \Delta C_{ac}$, $C_d = C_{0d} + \Delta C_d$, $R_d = R_{0d} + \Delta R_d$, where the subscript '0' denotes the nominal value; ΔL_g , ΔL_c , ΔC_{ac} , ΔC_d , ΔR_d are parameter variations around their nominal values. Therefore, Eq. (2) can be rearranged as:

$$\begin{cases} L_{0g}\dfrac{di_g}{dt} = R_{0d}(i_c - i_g) + \Delta R_d(i_c - i_g) - \Delta L_g\dfrac{di_g}{dt} - v_{cd} - v_{Cac} + v_{grid} \\ L_{0c}\dfrac{di_c}{dt} = R_{0d}(i_g - i_c) + \Delta R_d(i_g - i_c) - \Delta L_c\dfrac{di_c}{dt} + v_{cd} - v_o \\ C_{0ac}\dfrac{dv_{Cac}}{dt} = i_g - \Delta C_{ac}\dfrac{dv_{Cac}}{dt} \\ C_{0d}\dfrac{dv_{Cd}}{dt} = i_g - i_c - \Delta C_d\dfrac{dv_{Cd}}{dt} \end{cases} \tag{3}$$

Let

$$\begin{cases} f_1 = \Delta R_d(i_c - i_g) - \Delta L_g\dfrac{di_g}{dt} + v_{grid} + n_1 \\ f_2 = \Delta R_d(i_g - i_c) - \Delta L_c\dfrac{di_c}{dt} + n_2 \\ f_3 = -\Delta C_{ac}\dfrac{dv_{Cac}}{dt} + n_3 \\ f_4 = -\Delta C_d\dfrac{dv_{Cd}}{dt} + n_4 \end{cases} \tag{4}$$

where n_1, n_2, n_3 and n_4 represent unstructured uncertainties due to un-modeled dynamics. Then Eq.(3) can be expressed in the state-space equations:

$$\dot{\mathbf{x}} = \mathbf{A}_{\mathbf{c}0}\mathbf{x} + \mathbf{B}_{\mathbf{c}0}\mathbf{u} + \mathbf{G}_{\mathbf{c}0}\mathbf{f}\ ,\ \mathbf{y} = \mathbf{C}\mathbf{x} \tag{5}$$

where the vector of state variables $\mathbf{x} = [i_g, i_c, v_{Cac}, v_{cd}]^T$, the equivalent input vector $\mathbf{u} = [0, v_o, 0, 0]^T$, $\mathbf{f} = [f_1, f_2, f_3, f_4]^T$, and the nominal system matrices $\mathbf{A}_{\mathbf{c}0}$, $\mathbf{B}_{\mathbf{c}0}$, $\mathbf{G}_{\mathbf{c}0}$ and $\mathbf{C}$ are derived as:

$$\mathbf{A}_{\mathbf{c}0} = \begin{bmatrix} -\dfrac{R_{0d}}{L_{0g}} & \dfrac{R_{0d}}{L_{0g}} & -\dfrac{1}{L_{0g}} & -\dfrac{1}{L_{0g}} \\ \dfrac{R_{0d}}{L_{0c}} & -\dfrac{R_{0d}}{L_{0c}} & 0 & \dfrac{1}{L_{0c}} \\ \dfrac{1}{C_{0ac}} & 0 & 0 & 0 \\ \dfrac{1}{C_{0d}} & -\dfrac{1}{C_{0d}} & 0 & 0 \end{bmatrix}, \mathbf{B}_{\mathbf{c}0} = diag(0, -\frac{1}{L_{0c}}, 0, 0)\ ,$$

$$\mathbf{G}_{\mathbf{c}0} = diag(\frac{1}{L_{0g}}, \frac{1}{L_{0c}}, \frac{1}{C_{0ac}}, \frac{1}{C_{0d}})\ ,\ \mathbf{C} = diag(1, 0, 0, 0)$$

The transfer functions from the output of the voltage source inverter (VSI) to the grid-side current, converter-side current and the *RC*-filter brunch under nominal system parameters are derived as:

$$G_g(s)=\frac{I_g(s)}{V_o(s)}=\frac{R_{0d}s^2+\frac{1}{C_{0d}}s}{\{L_{0g}L_{0c}s^4+(L_{0g}+L_{0c})R_{0d}s^3+ [\frac{1}{C_{0d}}(L_{0g}+L_{0c})+\frac{L_{0c}}{C_{0ac}}]s^2+\frac{R_{0d}}{C_{0ac}}s+\frac{1}{C_{0ac}C_{0d}}\}} \tag{6}$$

$$G_c(s)=\frac{I_c(s)}{V_o(s)}=\frac{L_{0g}s^3+R_{0d}s^2+(\frac{1}{C_{0d}}+\frac{1}{C_{0ac}})s}{\{L_{0g}L_{0c}s^4+(L_{0g}+L_{0c})R_{0d}s^3 +[\frac{1}{C_{0d}}(L_{0g}+L_{0c})+\frac{L_{0c}}{C_{0ac}}]s^2+\frac{R_{0d}}{C_{0ac}}s+\frac{1}{C_{0ac}C_{0d}}\}} \tag{7}$$

$$G_{RC}(s)=\frac{I_{RC}(s)}{V_o(s)}=-\frac{L_{0g}s^3+\frac{1}{C_{0ac}}s}{\{L_{0g}L_{0c}s^4+(L_{0g}+L_{0c})R_{0d}s^3 +[\frac{1}{C_{0d}}(L_{0g}+L_{0c})+\frac{L_{0c}}{C_{0ac}}]s^2+\frac{R_{0d}}{C_{0ac}}s+\frac{1}{C_{0ac}C_{0d}}\}} \tag{8}$$

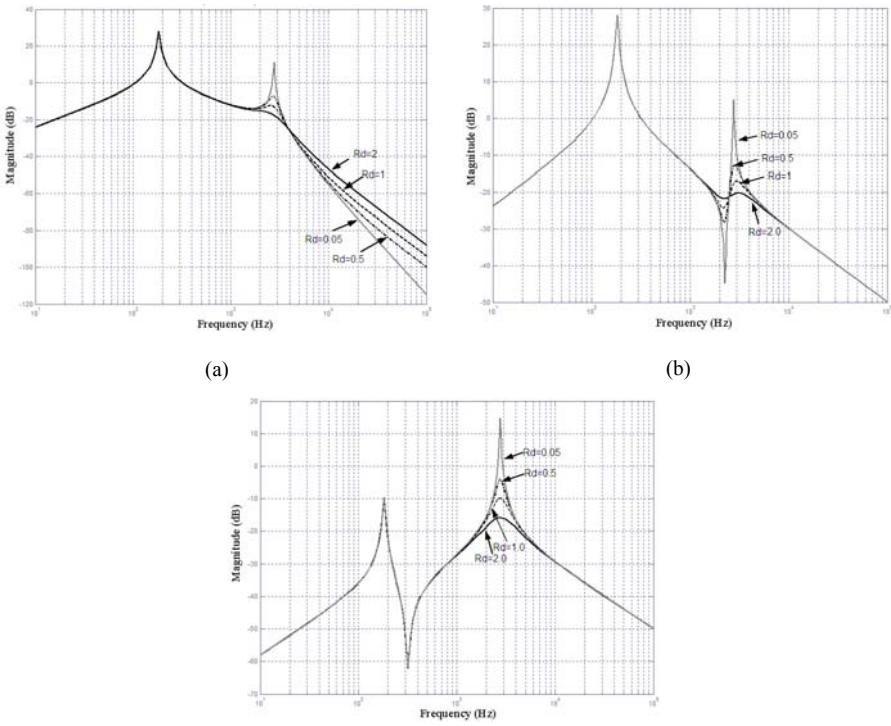
To provide an in-depth view of the frequency domain characteristics of Eqs. (6)-(8), the parameter design of the hybrid *LCL*-filter should be addressed, as reported in [27]. The major issues regarding the *LCL*-filter design include the total cost of inductors, the resonant frequency of the hybrid *LCL*-filter, the size of the damping resistance and the attenuation at the switching frequency in order to comply with the power quality standards imposed by IEEE 519-1992 and the IEC 61000-3-4 [4, 5]. In the present case, the resonant frequency at low frequency range is selected between the third and fifth order harmonic frequency to minimize the total cost of the hybrid filter. The next step is to design the *LCL*-filter parameters, which is the full order model of the *L*-filter model for the hybrid *LC*-filter design procedure. There are three major issues in designing of the *LCL*-filter parameters; namely, choosing the resonant frequency, the inductance ratio between the grid-side inductance (L_g) and converter-side inductance (L_c), and the selection of damping resistance [27]. The resonant frequency of the *LCL*-filter is selected significantly higher than the highest load harmonics compensated by the APF. And the selection of damping resistance is a compromise between the requirements of the stability margin and power dissipation. Further, the power quality standards should be rigorously studied to verify the designed parameters [4, 5]. Following these guidelines for parameter design, the specification and system parameters of the proposed hybrid APF is illustrated in Table 1.

Table 1
Specifications and system parameters

Name	Parameters
APF power rating	75 kVA (3-phase)
Nominal grid voltage (phase-to-phase)	380 V(RMS)
Ac-side capacitor C_{ac}	1000 μF
Grid-side inductor of the *LCL*-filter L_g	250 μH
Converter-side inductor of the *LCL*-filter L_c	500 μH
Ac capacitor of the *LCL*-filter C_d	10 μF
Damping resistance R_d	2 Ω
Dc-side voltage of the VSI	300 V
A/D sampling frequency	10 kHz
Inverter switching frequency	10 kHz

Fig. 2 shows the frequency responses of the hybrid *LCL*-filter corresponding to Eqs.(6)-(8), where the effect of damping resistance is also investigated. Fig. 2*a* indicates that the frequency response from inverter output $V_o(s)$ to the grid-side current of the *LCL*-filter $I_g(s)$ shows two resonant peaks, one in the low frequency range (185 Hz), another in the high frequency range (2.9 kHz). The resonant peak at low frequency range is caused by the *LC* resonance between the AC-side filter C_{ac} and the total inductance $L=L_g+L_c$. And the resonant peak at the high frequency range is caused by the *LC* resonance between the *RC*-filter (R_d and C_d) and the total inductance $L=L_g+L_c$. The damping resistance is found to have negligible effect on the resonant peak in the lower frequency range. However, smaller damping resistance causes significant resonant peak in the high frequency range, which implies that insufficient damping might cause instability of the system at higher frequencies. Fig. 2*b* shows the frequency response of the hybrid *LCL*-filter section from $V_o(s)$ to $I_c(s)$. A similar resonant frequency in the low frequency range is observed.

Whereas Fig. 2*b* shows two resonant peaks in the high frequency range, one shows the characteristic of overshoot and another shows the feature of undershoot. Fig. 2*b* also shows that smaller damping resistance results in higher resonant peaks in the high frequency range, making the system vulnerable due to poor stability margin. Fig. 2*c* shows the frequency response from inverter output $V_o(s)$ to the *RC*-filter brunch of the *LCL*-filter $I_{RC}(s)$. It shows that the resonant peak in the lower frequency range has an attenuation of -10dB, which implies that the lower frequency component generated by the VSI is damped in the *RC*-filter. However, the resonant peak in the high frequency range shows an attenuation of about 15 dB when the damping resistance is 0.05 Ω. It can also be inferred that smaller damping resistance results in current amplification at the *RC*-filter. Therefore, proper damping is mandatory to ensure the stable operation of the proposed system.



(a) (b)

(c)

Figure 2

Frequency response of the hybrid *LCL*-filter under different damping resistances. (a) From inverter output $V_o(s)$ to the grid-side current of the *LCL*-filter $I_g(s)$; (b) From inverter output $V_o(s)$ to the inverter-side current $I_c(s)$; (c) From inverter output $V_o(s)$ to the *RC*-filter brunch of the *LCL*-filter $I_{RC}(s)$

3 Control System Design

The current control loop is a key element for APFs. The cascaded controller structure is adopted for the proposed hybrid APF, which contains inner current-loop and outer dc-voltage loop (Fig. 3). The inner current loop is responsible for fast harmonic tracking and the outer loop is used for balancing the active power flow of the APF through regulating the dc-bus capacitor voltage [26, 27].

The adaptive linear neural network (ADALINE) is utilized as a harmonic identifier, which recursively extracts the amplitude and phase angle of an individual harmonic component by using the Widrow-Hopf learning algorithm [28]. By using the ADALINE algorithm, the compensating current of the APF is

reconstructed; thus, the control bandwidth is effectively reduced, and the stability margin imposed by the current tracking algorithm is ensured over a wide operation range. To enhance the performance of the APF, the feed-forward control algorithm is devised by feeding the non-active component of the load current into the feed-forward loop, and the voltage drop across the AC-side capacitor C_{ac} is utilized as the voltage feed-forward variable in the feed-forward control loop.

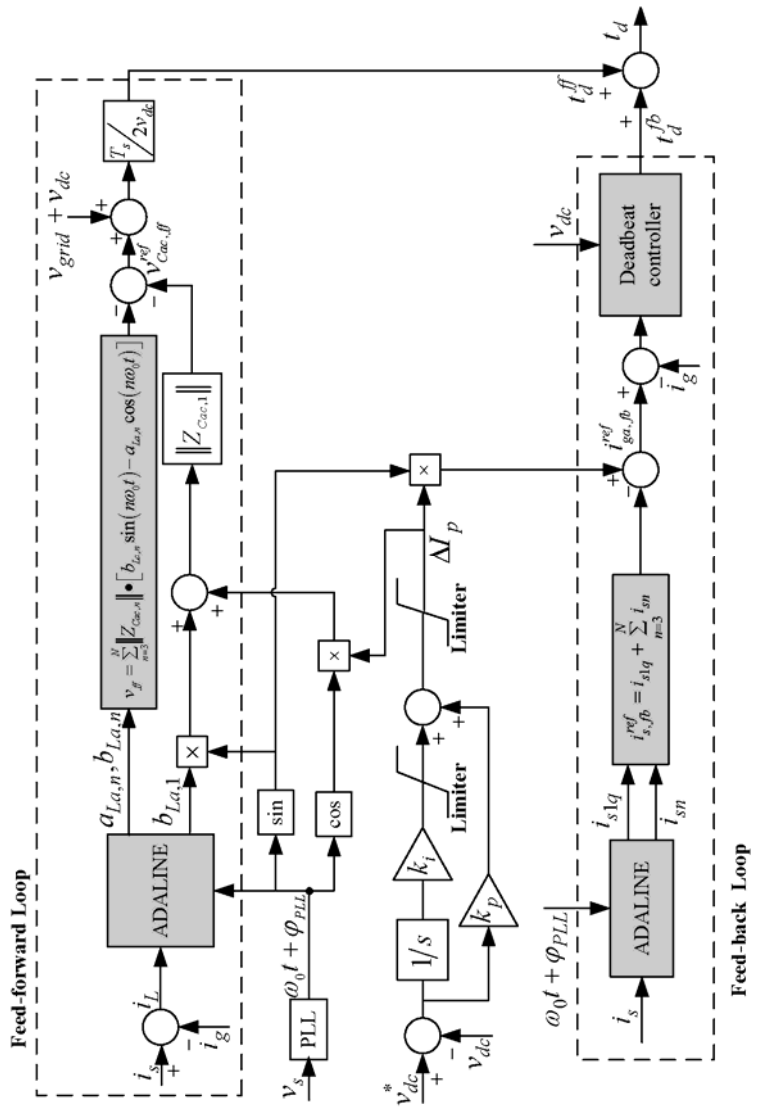


Figure 3
Control block diagram of the proposed hybrid LCL-filter based active power filter. (This figure is vertically presented for better clarity)

3.1 Harmonic Detection using Adaptive Linear Neural Network (ADALINE)

The most critical issues associated with APF control is that of finding an appropriate control algorithm, one which can obtain an accurate reference signal for control purposes, particularly when the load harmonics are time-varying [6-17]. Therefore, the performance of the APF strongly depends on the harmonic detection method [9-11]. To take advantage of the on-line learning capabilities of neural networks (NNs), the adaptive linear neural network (ADALINE) is utilized to estimate the time-varying magnitudes and phases of the fundamental and harmonic components from the source current and load current (Fig. 1) [6]. The motivation is to adopt a combined feed-forward and feedback control strategy for the proposed APF using ADALINEs as harmonic identifiers. For the sake of clarity, the background of ADALINE is briefly outlined herein [6, 28, 29].

An arbitrary signal $Y(t)$ at the kth sampling time can be represented by the Fourier series expansion as:

$$\begin{aligned} Y(t_k) &= \sum_{n=0,1,2,3,\cdots}^{N} A_n \sin(n\omega_0 t_k + \varphi_n) + \varepsilon(t_k) \\ &= \sum_{n=0,1,2,3,\cdots}^{N} (a_n \sin n\omega_0 t_k + b_n \cos n\omega_0 t_k) + \varepsilon(t_k) \end{aligned} \tag{9}$$

where A_n and φ_n are correspondingly amplitude and the phase angle of the nth order harmonic component, and $\varepsilon(t_k)$ represents higher order components and random noise, and a_n, b_n (n is integer) are also known as the Fourier coefficients, which can be calculated recursively using the least-mean-square (LMS) algorithm [30]. In other words, the Fourier coefficients can be estimated recursively by formulating the target signal $Y(t_k)$ as the inner product of the pattern vector X_k and weight vector W_k, which are defined as:

$$\begin{cases} X_k = [1, \sin\omega_0 t_k, \cos\omega_0 t_k, \cdots, \sin N\omega_0 t_k, \cos N\omega_0 t_k\ ]^T \\ W_k = [b_0^k, a_1^k, b_1^k, a_2^k, b_2^k, ..., a_N^k, b_N^k]^T \end{cases} \tag{10}$$

Therefore, the square error on the pattern X_k can be expressed as

$$\begin{aligned} \varepsilon_k &= \frac{1}{2}(d_k - X_k^T W_k)^2 = \frac{1}{2} e_k^2 \\ &= \frac{1}{2}(d_k^2 - 2d_k X_k^T W_k + W_k^T X_k X_k^T W_k) \end{aligned} \tag{11}$$

where d_k is the desired scalar output for the target signal $Y(t_k)$. The mean-square error (MSE) ε can be obtained by calculating the expectation of both sides of Eq. (12), as:

$$\varepsilon = E[\varepsilon_k] = \frac{1}{2}E[d_k^2] - E[d_k X_k^T]W_k + \frac{1}{2}W_k^T E[X_k X_k^T]W_k \tag{12}$$

where the weights are assumed to be fixed at W_k while computing the expectation. The objective of the ADALINE is to find optimal weight vector $\hat{W}_k$ that minimizes the MSE of Eq. (13). When mean-square error ε is minimized, the weight vector $\hat{W}$ after convergence would be [6, 28, 29]:

$$\hat{W} = [b_0, a_1, b_1, a_2, b_2, ..., a_N, b_N]^{\mathrm{T}} \tag{13}$$

Thus, the fundamental component and the *n*th order harmonic component of the measured signal can be obtained as:

$$\begin{cases} Y_1(t_k) = a_1 \sin(\omega_0 t_k) + b_1 \cos(\omega_0 t_k) \\ Y_n(t_k) = a_n \sin(n\omega_0 t_k) + b_n \cos(n\omega_0 t_k) \end{cases} \tag{14}$$

In this paper, the fixed-point digital signal processors (DSPs) from Texas Instruments (TI TMS320F2812) are adopted to implement the ADALINE-based estimation algorithm and the control algorithm for the APF. The phase and magnitude of the individual harmonic components, from the 3rd to the 25th order, are estimated for the higher convergence of ADALINE, but only the lower-order harmonics from 3rd to 19th order are selected in the current-loop control to save the computation resources. However, the selected harmonics can easily be extended. The accurate and rapid estimation capability of ADALINE is crucial when selective harmonic compensation is adopted in current control for the purpose of reducing controller bandwidth, thus increasing system robustness and enhancing stability [28].

3.2 The Proposed Feedback plus Feed-forward Control Strategy

In this section, the feedback plus feed-forward control scheme are described consecutively. Firstly, the deadbeat control law for the average current control scheme is introduced by using the discrete domain representation of the *LCL*-filter model. Then, stability analysis of the closed-loop current control schemes under various parameter variation scenarios is presented. Finally, the feed-forward control loop, which achieves fast load disturbance compensation, is presented.

In the forthcoming derivations, the current in phase '*a*' is analyzed for the sake of brevity. However, the same conclusions can also be applied for the other phases. The load current in phase '*a*' is represented by:

$$
\begin{aligned}
& i_{La}(t) = \sum_{n=1}^{\infty} I_{La,n} \sin(n\omega_0 t + \varphi_{La,n}) \\
& = a_{La,1} \sin(\omega_0 t + \varphi_{PLL}) + b_{La,1} \cos(\omega_0 t + \varphi_{PLL}) \\
& + \sum_{n=2}^{\infty} [a_{La,n} \sin(n\omega_0 t) + b_{La,n} \cos(n\omega_0 t)]
\end{aligned} \tag{15}
$$

where $a_{La,1}=I_{La,1}\cos(\varphi_{La,1}-\varphi_{PLL})$ and $b_{La,1}=I_{La,1}\sin(\varphi_{La,1}-\varphi_{PLL})$ represent the amplitude of the fundamental active and reactive component of the nonlinear load current, and φ_{PLL} represents the initial phase angle of the phase-locked-loop (PLL) [28, 29], which is synchronized with the fundamental frequency component of the grid voltage. And $I_{La,n}$ and $\varphi_{La,n}$ (n>1, n is integer) represent the amplitude and phase angle of the nth order harmonic component of the load current, respectively. The parameters $a_{La,n}$ and $b_{La,n}$ (n>1, n is integer) represent the weights of the individual harmonic component obtained from the ADALINE. The individual harmonic component can be reconstructed using Eq. (15) if the weights $a_{La,n}$ and $b_{La,n}$ (n is integer) are precisely calculated. Similarly, the source-side current in phase 'a' supplied by the distribution system is represented as:

$$
\begin{aligned}
& i_{sa}(t) = a_{sa,1} \sin(\omega_0 t + \varphi_{PLL}) + b_{sa,1} \cos(\omega_0 t + \varphi_{PLL}) \\
& + \sum_{n=2}^{\infty} [a_{sa,n} \sin(n\omega_0 t) + b_{sa,n} \cos(n\omega_0 t)]
\end{aligned} \tag{16}
$$

where $a_{sa,1}= I_{sa,1}\cos(\varphi_{sa,1}-\varphi_{PLL})$ and $b_{sa,1}=I_{sa,1}\sin(\varphi_{sa,1}-\varphi_{PLL})$ represent the amplitude of the fundamental active and reactive component of the source-side current, and $I_{sa,n}$ and $\varphi_{sa,n}$ (n>1, n is integer) represent the amplitude and phase angle of the nth order harmonic component of the source-side current, respectively. The parameters $a_{sa,n}$ and $b_{sa,n}$ (n is integer) represent the weights of the individual harmonic component obtained from a separate ADALINE block in the feedback loop (Fig. 3). To achieve the feedback current tracking control, the fundamental reactive component and the selected harmonic components are utilized as the reference current for the APF. Furthermore, the output of the voltage-loop controller ΔI_p, after being multiplied by a unit sinusoidal signal synchronized with the grid voltage by using PLL, is added to the feedback current to compensate for the power loss of the inverter [6-19]. Therefore, the compensating current of the APF in the feedback loop is represented as:

$$
\begin{aligned}
& i_{ga,fb}^{ref}(t) = -\{b_{sa,1} \cos(\omega_0 t + \varphi_{PLL}) + \sum_{n=3}^{N} [a_{sa,n} \sin(n\omega_0 t) + b_{sa,n} \cos(n\omega_0 t)]\} \\
& + \Delta I_p \sin(\omega_0 t + \varphi_{PLL})
\end{aligned} \tag{17}
$$

Note that a finite number of harmonics is selected in Eq. (17), since only a limited number of harmonics are processed in the ADALINE-based harmonic estimation scheme due to the limited computational load, constrained by the DSP.

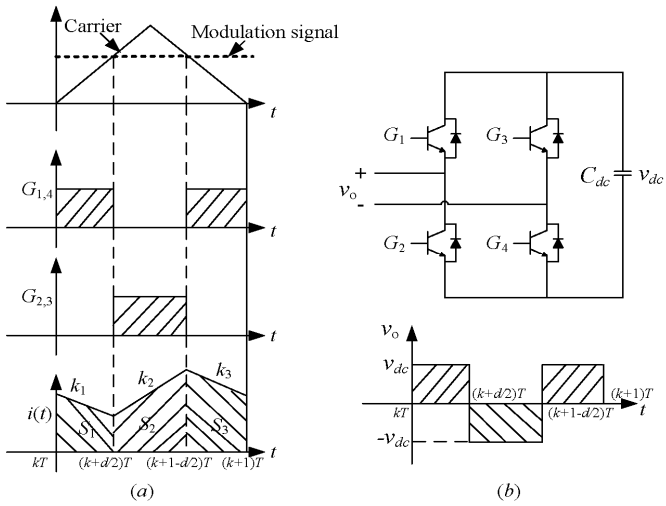


Figure 4

Principle of current tracking control scheme: (a) Geometrical interpretation for deriving the average current during one PWM period; (b) Schematic of the voltage source inverter (VSI) and its output voltage

3.2.1 Deadbeat Control Scheme for the Feedback Current Control Loop

To simplify the control effort for the proposed hybrid APF, the deadbeat control scheme is adopted in the feedback closed-loop for reference current tracking. Only the *LCL*-section of the hybrid APF is used to derive the deadbeat control law. The AC-side capacitor voltage, on the other hand, is regulated by controlling the injection current of the *LCL*-filter. Moreover, the *RC*-filter brunch of the *LCL*-filter section, adopted for high frequency switching ripple attenuation and stability enhancement, shows little impact on the low frequency range below 2 kHz (Fig. 2*a*). Hence, the effect of the *RC*-filter is neglected when deriving the deadbeat control law for the sake of simplicity. Therefore, the degree of freedom of the control system for the hybrid APF is significantly reduced.

Utilizing the concept of the reduced order model for the *LCL*-filter, the deadbeat current control law for the inner current loop is derived herein. Firstly, the differential equation for the inductor current across *LCL*-filter section is represented as:

$$v_{grid} - v_{Cac} - v_o = \left(L_g + L_c\right)\frac{di}{dt} \tag{18}$$

where parameters v_{grid}, v_{Cac} and v_o represent the grid side voltage, the AC-capacitor voltage and output voltage of the voltage source inverter, respectively. In order to derive the discrete domain representation of Eq. (18), the operation

principle of the inverter under different switching patterns is given by Fig. 4. It can be observed that, when the switches G_1 and G_4 are switched on, and the switches G_2 and G_3 are turned off, the output voltage of the inverter is v_{dc}, and then the inverter current undergoes a falling stage, according to the direction of current defined in Fig. 1. When the switches G_1 and G_4 are switched off, and switches G_2 and G_3 are switched on, the output voltage of VSI would be $-v_{dc}$, which results in a rising stage of the inverter current (Fig. 4*a*-*b*). Therefore, Eq. (18) can be rewritten in the discrete form using piecewise linear representation as:

$$\begin{cases} i_g[(k+\frac{d}{2})T_s]-i_g[kT_s]=\frac{d}{2}T_s\cdot\frac{v_{grid}[k]-v_{Cac}[k]-v_{dc}[k]}{L_g+L_c} \\ i_g[(k+1-\frac{d}{2})T_s]-i_g[(k+\frac{d}{2})T_s]=(1-d)T_s\cdot\frac{v_{grid}[k]-v_{Cac}[k]+v_{dc}[k]}{L_g+L_c} \\ i_g[(k+1)T_s]-i_g[(k+1-\frac{d}{2})T_s]=\frac{d}{2}T_s\cdot\frac{v_{grid}[k]-v_{Cac}[k]-v_{dc}[k]}{L_g+L_c} \end{cases} \tag{19}$$

where d in Eq. (19) is the abbreviation of $d[k]$, representing the duty cycle of the kth control period. The grid voltage and AC capacitor voltage are assumed to be constants during one PWM cycle (quasi-steady-state model) in discrete equations. After mathematical manipulations of Eq. (19), the duty ratio of PWM signal at the kth control period is obtained as:

$$d[k]=-\frac{(L_g+L_c)\{i_g[(k+1)T_s]-i_g[kT_s]\}}{2v_{dc}[k]T_s}+\frac{v_{dc}[k]+v_{grid}[k]-v_{Cac}[k]}{2v_{dc}[k]} \tag{20}$$

In order to track the reference signal and achieve deadbeat control, the current at (k+1)th sampling interval $i_g[(k+1)T_s]$ should be replaced by the reference signal at the next sampling cycle [26, 31]. Nevertheless, in the proposed hybrid APF, the resetting filters are adopted at the sampling stage, and hence the instantaneous quantities cannot be directly obtained at kth and (k+1)th sampling instants. On the contrary, all the sampling signals, i.e., the voltages and currents, are the average quantities of the previous period. Therefore, the current tracking scheme should be modified to account for the average quantities, and hence the theoretical derivation of the average current during the kth control period is given herein.

Referring to Fig. 4*a*, it can be deduced that, during the switching on/off processes of the power electronic switches, the output current during one control period undergoes rising and falling stages according to the switching patterns of the switches. Therefore, the average current can be obtained by dividing the total shadowed area denoted as S_1, S_2 and S_3 by the control period T_s. As shown in Fig. 4*a*, the slopes of the current $i(t)$ during one PWM control period are denoted as:

$$\begin{cases} k_1 = k_3 = \dfrac{v_{grid}[k] - v_{Cac}[k] - v_{dc}[k]}{L_g + L_c} \\ k_2 = \dfrac{v_{grid}[k] - v_{Cac}[k] + v_{dc}[k]}{L_g + L_c} \end{cases} \tag{21}$$

The shadowed area denoted as S_1, S_2 and S_3 in Fig. 4*a* can be derived as:

$$\begin{cases} S_1 = \dfrac{1}{2}\{2i_g[kT_s] + k_1 \dfrac{d}{2}T_s\} \cdot \dfrac{d}{2}T_s \\ S_2 = \dfrac{1}{2}\{2i_g[kT_s] + k_1 dT_s + k_2(1-d)T_s\} \cdot (1-d)T_s \\ S_3 = \dfrac{1}{2}\{2i_g[kT_s] + k_1 \cdot \dfrac{3d}{2}T_s + 2k_2(1-d)T_s\} \cdot \dfrac{d}{2}T_s \end{cases} \tag{22}$$

Therefore, the average inverter current of the *k*th control period can be derived as:

$$\overline{i_g}[kT_s] = \frac{S_1 + S_2 + S_3}{T_s} \tag{23}$$

Therefore, from Eqs. (22) and (23), the instantaneous current at the (*k*+1)th sampling instant can be rewritten as:

$$i_g[(k+1)T_s] = \overline{i_g}[kT_s] + \frac{\{v_{dc}[k] + v_{grid}[k] - v_{Cac}[k]\}T_s - 2dT_s v_{dc}[k]}{2(L_g + L_c)} \tag{24}$$

Hence, the duty cycle can be rewritten in terms of the average current of the *k*th sampling period as:

$$d[k] = -\frac{(L_g + L_c)\{i_g[(k+1)T_s] - \overline{i_g}[kT_s]\}}{v_{dc}[k]T_s} + \frac{v_{dc}[k] + v_{grid}[k] - v_{Cac}[k]}{2v_{dc}[k]} \tag{25}$$

In Eq. (25), the term L/T_s is denoted as the current controller gain derived from the deadbeat control law. It is interesting to notice from Eq. (20) and Eq. (25) that the deadbeat control law for the average current tracking control and the instantaneous current tracking control have similar expression. However, the controller gain, denoted by L/T_s, for the current tracking error in Eq. (25) of the average current tracking scheme is twice the value of the instantaneous current tracking scheme, which shows the superior performance for the proposed scheme; i.e., the adoption of resetting filter is helpful in increasing the current controller gain, thus increasing the tracking dynamics for the reference compensation current of the APF.

Nevertheless, the aforementioned deadbeat control scheme is based on the reduced order model of the *LCL*-filter, where the *RC*-filter is neglected at the modeling stage. Hence, the performance of the current tracking scheme may be imperfect

due to model mismatch and parameter uncertainty. Therefore, the stability analysis of the current control scheme is rigorously studied to ensure the stable operation of the APF. In the forthcoming subsection, the *RC*-filter is incorporated into the mathematical manipulations and the selection of the current controller gain is discussed with respect to the stability requirement.

3.2.2 Root Locus Analysis of the Grid-side Current Tracking Scheme

This subsection presents the performance of the grid-side current (i_g) tracking scheme by using the closed-loop root locus plots and the open-loop impulse responses. The plant model under this scenario can be obtained by deriving the open-loop transfer function from the inverter output to the grid-side current of the *LCL*-filter section:

$$G_{g,plant}(s) = \frac{R_{0d}C_{0d}s + 1}{L_{0g}L_{0c}C_{0d}s^3 + R_{0d}C_{0d}(L_{0g} + L_{0c})s^2 + (L_{0g} + L_{0c})s} \tag{26}$$

The current loop transfer function $G_{g,cc}(s)$ is simply represented by a proportional gain K_{cc}, and the transfer function of the delay due to PWM generation and computational delay (T_d) is expressed as:

$$G_{g,delay}(s) = e^{-sT_d} \tag{27}$$

Hence the open loop transfer function of the grid-side current tracking control algorithm can be represented by:

$$\begin{aligned} G_{g,open}(s) &= G_{g,cc}(s)G_{g,plant}(s)G_{g,delay}(s) \\ &= K_{cc}e^{-sT_d}\frac{R_{0d}C_{0d}s + 1}{L_{0g}L_{0c}C_{0d}s^3 + R_{0d}C_{0d}(L_{0g} + L_{0c})s^2 + (L_{0g} + L_{0c})s} \end{aligned} \tag{28}$$

Therefore, the closed-loop transfer function of the grid-side current tracking control scheme can be derived as:

$$\begin{aligned} G_{g,close}(s) = \frac{G_{g,open}(s)}{1 + G_{g,open}(s)} = \frac{K_{cc}e^{-sT_d}(R_{0d}C_{0d}s + 1)}{\{L_{0g}L_{0c}C_{0d}s^3 + R_{0d}C_{0d}(L_{0g} + L_{0c})s^2} \\ +(K_{cc}R_{0d}C_{0d}e^{-sT_d} + L_{0g} + L_{0c})s + K_{cc}e^{-sT_d}\} \end{aligned} \tag{29}$$

It should be noted that, to achieve an optimal dynamic performance of the proposed hybrid APF, the selection of the current loop controller should be rigorously studied. If the gain is selected too small, the dynamic response of the current tracking will be sluggish. On the other hand, if the current loop gain is too high, the stability constraint of the closed-loop control will be violated. Hence the current loop gain will be carefully studied in the subsection by using discrete domain representation of the closed-loop transfer function under various parameter variation scenarios, which will be discussed herein.

Referring to Eq. (29), the closed-loop transfer function of the current loop tracking control under nominal system parameters can be rewritten in the discrete domain (z-domain) as:

$$G_{g,close}(z)=\frac{K_{cc}(0.08836z^2+0.09784z-0.004811)}{\{z^4-0.9407z^3+(0.08836K_{cc}+0.2419)z^2 \\ +(0.09784K_{cc}-0.3012)z-0.004811K_{cc}\}} \tag{30}$$

where T_d is assumed to be one control period (T_s=100μs). The closed-loop root locus plot and open-loop impulse response of the grid-side current control scheme under nominal system parameters is illustrated by Fig. 5*a*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 5.6. It is interesting to notice that this stability margin is lower than the controller gain directly derived from the deadbeat control low. This gain limit should be satisfied in the practical system to ensure closed-loop stability, as discussed in the simulation and experimental results. Moreover, it can be observed from Fig. 5*a* that the open-loop impulse response shows an overshoot of 0.18 p.u with the response time of 1.2 millisecond. In order to investigate the robustness of the presented hybrid APF and the control scheme, the influence of parameter variations is also rigorously studied herein by taking into account the variation of interfacing inductances, the control delay and the *RC* filter parameter variations.

It should be noted that the interfacing inductances may deviate from their nominal values in practical systems due to the variation of the operational conditions, humidity and temperature deviation. Hence the influence of inductance variations is considered here by changing the grid-side inductance to 0.8 p.u and converter side inductance to 1.2 p.u. Under this condition, the closed-loop transfer function of the grid-side current tracking scheme in discrete domain can be derived as:

$$G_{g,close}(z)=\frac{K_{cc}(0.09322z^2+0.1047z-0.00515)}{\{z^4-0.9617z^3+(0.09322K_{cc}+0.2731)z^2 \\ +(0.1047K_{cc}-0.3114)z-0.00515K_{cc}\}} \tag{31}$$

The closed-loop root locus plot and open-loop impulse response of the grid-side current tracking scheme under inductance variations is illustrated by Fig. 5*b*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 5.15, which is lower than the case of the nominal system parameters. Besides, it can be observed from Fig. 5*b* that the open-loop impulse response shows an overshoot of 0.195 p.u with the response time of 1.2 millisecond. Next, we consider the effect of the control delay on the performance of the current tracking control, which is associated with PWM generation and computational delay, etc. Considering the control delay as $1.5T_s$, then the closed-loop transfer function of the current tracking algorithm is derived as:

$$G_{g,close}(z) = \frac{K_{cc}(0.02253z^3 + 0.1347z^2 + 0.02834z - 0.00414)}{\{z^5 - 0.9407z^4 + (0.02253K_{cc} + 0.2419)z^3 + (0.1347K_{cc} - 0.3012)z^2 + 0.02834K_{cc}z - 0.00414K_{cc}\}} \quad (32)$$

The closed-loop root locus plot and open-loop impulse response of the grid-side current tracking scheme corresponding to the variation of control delay is illustrated by Fig. 5*c*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 4.87, which is lower than the case of the nominal system parameters. Besides, it can be observed from Fig. 5*c* that the open-loop impulse response shows an overshoot of 0.17 p.u with the response time of 1.2 millisecond, which is almost the same as the case of the nominal system parameters. It is also found that a longer delay would not only deteriorate the stability of the closed-loop system, but would also significantly hamper the quality of the output voltage waveform, which would result in poor precision of the current tracking algorithm. However, as discussed in the experimental results, the control delay does not have a significant effect on the performance of the system since the ADALINE-based harmonic estimation algorithm was adopted to generate the reference current for the current loop controller. Hence the control delay can be compensated for by shifting the reference compensation current of the APF by one sampling period, which can be easily achieved by adding $\Delta\theta_n$ ($\Delta\theta_n=\omega_n T_s=2\pi f_0 n T_s$, n is the harmonic order) to the phase angle of the individual harmonic component by modifying the $sin(n\omega_0 t)$ and $cos(n\omega_0 t)$ into $sin(n\omega_0 t+\Delta\theta_n)$ and $cos(n\omega_0 t+\Delta\theta_n)$ in the reconstruction process of the ADALINE-based harmonic estimation algorithm.

Next, we consider the effect of the *RC*-filter parameters on the performance of the current loop tracking algorithm by changing the filtering capacitance and the damping resistance, respectively. If the filtering capacitance of the *RC*-filter is modified to C_d=5 μF, then the closed-loop transfer function of the current tracking control algorithm is derived as:

$$G_{g,close}(z) = \frac{K_{cc}(0.1391z^2 + 0.1296z + 0.04588)}{\{z^4 + 0.05781z^3 + (0.1391K_{cc} - 0.7566)z^2 + (0.1296K_{cc} - 0.3012)z + 0.04588K_{cc}\}} \quad (33)$$

The closed-loop root locus plot and open-loop impulse response of the grid-side current tracking control with the variation of filtering capacitance is illustrated by Fig. 5*d*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 7.66, which is much higher than the case of the nominal system parameters. Moreover, it can be observed from Fig. 5*d* that the open-loop impulse response shows an overshoot of 0.144 p.u with the response time of 1.1 millisecond, which is remarkably lower than the case of nominal system parameters. It is found that the smaller the filtering capacitance, the higher the stability margin and the faster the dynamic response of the current tracking

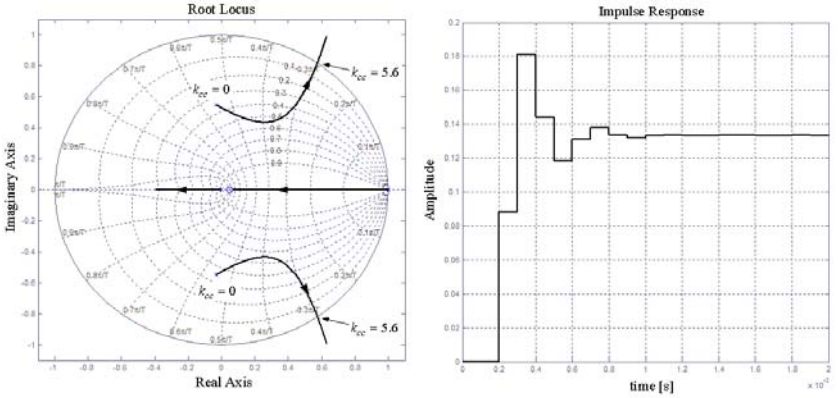
control algorithm can be achieved. Nevertheless, smaller filtering capacitance would result in poor attenuation of higher order switching harmonics. Therefore, a compromise should be achieved between the filtering efficiency and the closed-loop stability constraint. Next, the effect of the damping resistance on the closed-loop current tracking control is examined by changing the damping resistance R_d to 0.1Ω, and then the closed-loop transfer function can be derived as:

$$G_{g,close}(z) = \frac{K_{cc}(0.05958z^2 + 0.189z + 0.05182)}{\{z^4 - 0.6889z^3 + (0.05958K_{cc} + 0.6306)z^2 + (0.189K_{cc} - 0.9418)z + 0.05182K_{cc}\}} \quad (34)$$

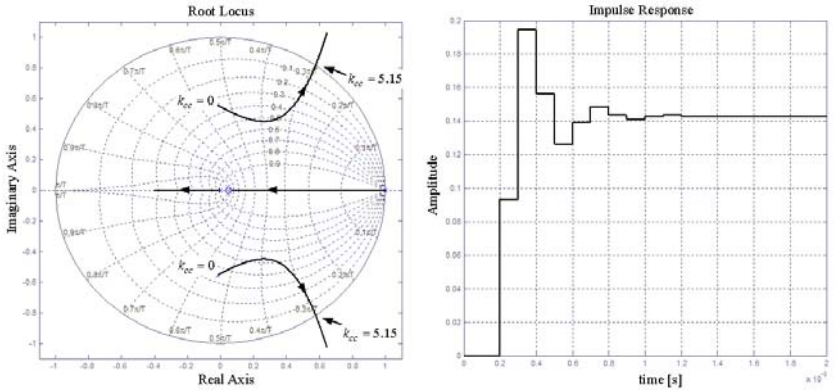
The closed-loop root locus plot and open-loop impulse response of the grid-side current tracking control scheme with the variation of damping resistance is illustrated by Fig. 5*e*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 5.29, which is lower than the case of the nominal system parameters. Besides, it can be observed from Fig. 5*e* that the open-loop impulse response shows an overshoot of 0.23 p.u with the response time of 18 millisecond, which is significantly higher than the case of the nominal system parameters. It is found that a smaller damping resistance would result in a smaller stability margin and a prolonged dynamic response of the current tracking control scheme. On the other hand, however, the reduced damping resistance results in a higher damping of higher order switching harmonics of the inverter, as demonstrated in Fig. 2*a*. Therefore, a compromise must be achieved between the stability constraint and the switching ripple attenuation for practical systems. Table 2 shows the summery of the stability margin and dynamic response of the grid-side current tracking control scheme, where the results obtained under the nominal system parameters and parameter variation scenarios are presented. In the forthcoming subsection, a similar analysis is provided for the closed-loop locus diagrams and open-loop impulse responses of the current regulation scheme based on the converter-side tracking control scheme.

Table 2
Summary of the stability margin and dynamic response of the grid-side current tracking scheme

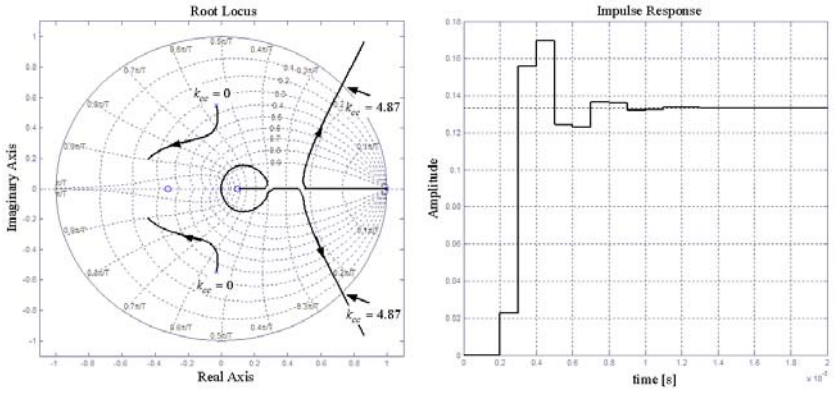
Case	Marginal gain (deg)	Overshoot (pu)	Response time (ms)
1	5.6	0.18	1.2
2	5.15	0.195	1.2
3	4.87	0.17	1.2
4	7.76	0.144	1.1
5	5.29	0.23	18


Root Locus
Imaginary Axis
Real Axis
$k_{cc} = 0$
$k_{cc} = 5.6$
$k_{cc} = 0$
$k_{cc} = 5.6$
Impulse Response
Amplitude
time [s]

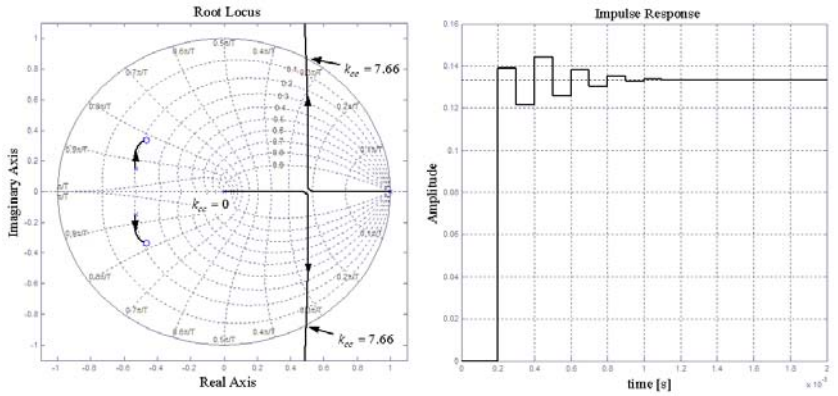
(a)


Root Locus
Imaginary Axis
Real Axis
$k_{cc} = 0$
$k_{cc} = 5.15$
$k_{cc} = 0$
$k_{cc} = 5.15$
Impulse Response
Amplitude
time [s]

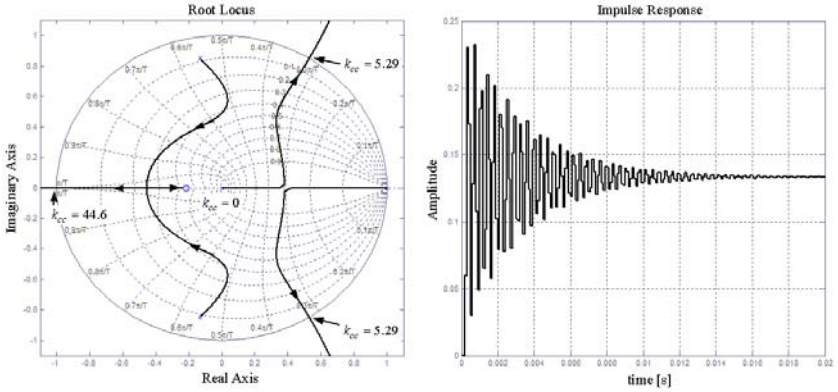
(b)


Root Locus
Imaginary Axis
Real Axis
$k_{cc} = 0$
$k_{cc} = 4.87$
$k_{cc} = 0$
$k_{cc} = 4.87$
Impulse Response
Amplitude
time [s]

(c)



(d)



(e)

Figure 5

The closed-loop root locus diagrams and the open-loop impulse responses of the current regulation algorithm based on the grid-side current (i_g) tracking control scheme. (a) Root locus and impulse response under nominal parameters; (b) Root locus and impulse response under inductance variations; (c) Root locus and impulse response under different control delay (T_d=1.5T_s); (d) Root locus and impulse response under different *RC*-filter capacitance C_d; (e) Root locus and impulse response under different *RC*-filter resistance R_d

3.2.3 Root Locus Analysis of the converter-side Current Tracking Scheme

This subsection presents the performance of the converter-side current (i_c) tracking scheme by using the closed-loop root locus plots and the open-loop impulse responses. The plant model under this scenario can be obtained by deriving the open-loop transfer function from the inverter output to the converter side current of the *LCL*-filter section:

$$G_{c,plant}(s) = \frac{L_{0g}C_{0d}s^2 + R_{0d}C_{0d}s + 1}{L_{0g}L_{0c}C_{0d}s^3 + R_{0d}C_{0d}(L_{0g} + L_{0c})s^2 + (L_{0g} + L_{0c})s} \tag{35}$$

The current loop transfer function $G_{c,cc}(s)$ is simply represented by a proportional gain K_{cc}, and the transfer function of the delay due to PWM generation and computational delay is derived as:

$$G_{c,delay}(s) = e^{-sT_d} \tag{36}$$

Hence the open loop transfer function of the converter-side current tracking control algorithm under the present case can be represented by:

$$G_{c,open}(s) = K_{cc}e^{-sT_d}\frac{L_{0g}C_{0d}s^2 + R_{0d}C_{0d}s + 1}{L_{0g}L_{0c}C_{0d}s^3 + R_{0d}C_{0d}(L_{0g} + L_{0c})s^2 + (L_{0g} + L_{0c})s} \tag{37}$$

Therefore, the closed-loop transfer function of the converter-side current tracking control scheme is:

$$G_{c,close}(s) = \frac{G_{c,open}(s)}{1 + G_{c,open}(s)} = \frac{K_{cc}e^{-sT_d}(L_{0g}C_{0d}s^2 + R_{0d}C_{0d}s + 1)}{\{L_{0g}L_{0c}C_{0d}s^3 + [K_{cc}e^{-sT_d}L_{0g}C_{0d} + R_{0d}C_{0d}(L_{0g} + L_{0c})]s^2 + (K_{cc}R_{0d}C_{0d}e^{-sT_d} + L_{0g} + L_{0c})s + K_{cc}e^{-sT_d}\}} \tag{38}$$

The closed-loop transfer function of the converter-side current tracking scheme can be rewritten in the discrete domain, which will be discussed in detail herein. Under nominal system parameters, the closed-loop transfer function of the converter-side current (i_c) tracking control scheme can be rewritten in the discrete domain (z-domain):

$$G_{c,close}(z) = \frac{K_{cc}(0.1558z^2 - 0.03707z + 0.6264)}{\{z^4 - 0.9407z^3 + (0.1558K_{cc} + 0.2419)z^2 - (0.03707K_{cc} + 0.3012)z + 0.6264K_{cc}\}} \tag{39}$$

where T_d is assumed to be one control period (T_s=100μs). The closed-loop root locus and open-loop impulse response of the converter-side current tracking scheme corresponding to the nominal system parameters is illustrated by Fig. 6*a*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 9.91. It is worth noting that this stability margin is higher than the controller gain directly derived from the deadbeat control low. On the other hand, however, this gain is also higher than the stability margin obtained from the grid-side current tracking control scheme. Moreover, it can be observed from Fig. 6*a* that the open-loop impulse response shows an overshoot of 0.155 p.u with the response time of 1.2 millisecond.

Next, the influence of parameter variations is also rigorously studied herein by taking into account the variation of interfacing inductances, the control delay and the *RC*-filter parameter variations. Similar to the previous section, the influence of inductance variations is considered here by changing the grid-side inductance to 0.8 p.u and converter-side inductance to 1.2 p.u. Under this condition, the closed-loop transfer function in discrete domain can be derived as:

$$G_{c,close}(z)=\frac{K_{cc}(0.1801z^2-0.06898z+0.08171)}{\{z^4-0.9617z^3+(0.1801K_{cc}+0.2731)z^2 \\ -(0.06898K_{cc}+0.3114)z+0.08171K_{cc}\}} \tag{40}$$

The closed-loop root locus and open-loop impulse response of the converter-side current tracking scheme corresponding to inductance variations is illustrated by Fig. 6*b*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 8.79, which is lower than the case of the nominal system parameters. Besides, it can be observed from Fig. 6*b* that the open-loop impulse response shows an overshoot of 0.18 p.u with the response time of 1.4 millisecond. Next, we consider the effect of control delay on the performance of the converter-side current tracking scheme. Similar to the previous section, here the control delay is considered to be $1.5T_s$; then the closed-loop transfer function of the current tracking algorithm is derived as:

$$G_{c,close}(z)=\frac{K_{cc}(0.08873z^3+0.0386z^2+0.02188z+0.3219)}{\{z^5-0.9407z^4+(0.08873K_{cc}+0.2419)z^3 \\ +(0.0386K_{cc}-0.3012)z^2+0.02188K_{cc}z+0.3219K_{cc}\}} \tag{41}$$

The closed-loop root locus and open-loop impulse response of the converter-side current tracking scheme corresponding to the variation of control delay is illustrated by Fig. 6*c*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 7.48, which is lower than the case of the nominal system parameters. Besides, it can be observed from Fig. 6*c* that the open-loop impulse response shows an overshoot of 0.138 p.u with the response time of 1.2 millisecond, which exhibits lower overshoot than the case of the nominal system parameters. Next, we consider the effect of the *RC* filter parameters on the performance of the converter-side current control scheme by changing the filtering capacitance and the damping resistance, respectively. If the filtering capacitance of the *RC* filter is modified to C_d=5 μF, then the closed-loop transfer function of the converter-side current tracking control algorithm is derived as:

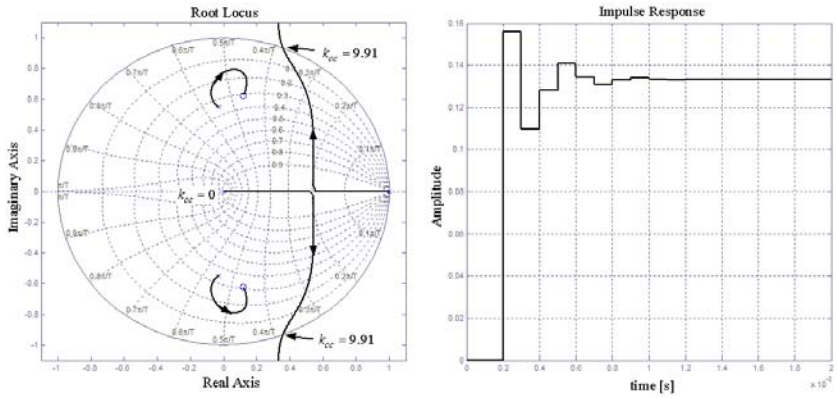
$$G_{c,close}(z)=\frac{K_{cc}(0.1305z^2+0.1468z+0.0373)}{\{z^4+0.05781z^3+(0.1305K_{cc}-0.7566)z^2 \\ +(0.1468K_{cc}-0.3012)z+0.0373K_{cc}\}} \tag{42}$$

The closed-loop root locus and open-loop impulse response of the converter-side current control scheme with the variation of filtering capacitance is illustrated by Fig. 6*d*. It can be observed that the closed-loop system would be unstable when the current controller gain exceeds 7.46, which is much higher than the case of the nominal system parameters. Moreover, it can be observed from Fig. 6*d* that the open-loop impulse response shows an overshoot of 0.14 p.u with the response time of 1.1 millisecond, which is remarkably lower than the case of the nominal system parameters. It is worth noting that, the smaller the filtering capacitance, the lower is the achieved stability margin of the current tracking control algorithm, which shows a phenomenon the reverse of the case of the grid-side current tracking control scheme. Next, the effect of the damping resistance on the closed-loop current tracking control is examined by changing the damping resistance R_d to 0.1 Ω, and then the closed-loop transfer function can be derived as:

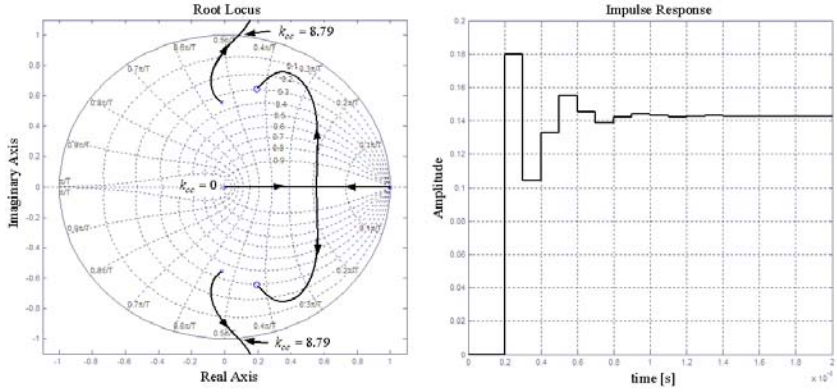
$$G_{c,close}(z) = \frac{K_{cc}(0.1702z^2 - 0.3227z + 0.1624)}{\{z^4 - 0.6889z^3 + (0.1702K_{cc} + 0.6306)z^2 - (0.3227K_{cc} + 0.9418)z + 0.1624K_{cc}\}} \tag{43}$$

The closed-loop root locus plot and open-loop impulse response of the converter-side current tracking control scheme with the variation of damping resistance is illustrated by Fig. 6*e*. It can be observed that the closed-loop system shows multiple poles at the unit cycle of the root locus diagram, and the system would be unstable when the current controller gain exceeds 1.09, which is significantly lower than in the case of the nominal system parameters. Besides, it can be observed from Fig. 6*e* that the open-loop impulse response shows an overshoot of 0.185 p.u with the response time of 18 millisecond, which is significantly higher than in the case of nominal system parameters. It is found that smaller damping resistance would result in smaller stability margin and prolonged dynamic response of the converter-side current control scheme, which is consistent with the analysis in the previous section.

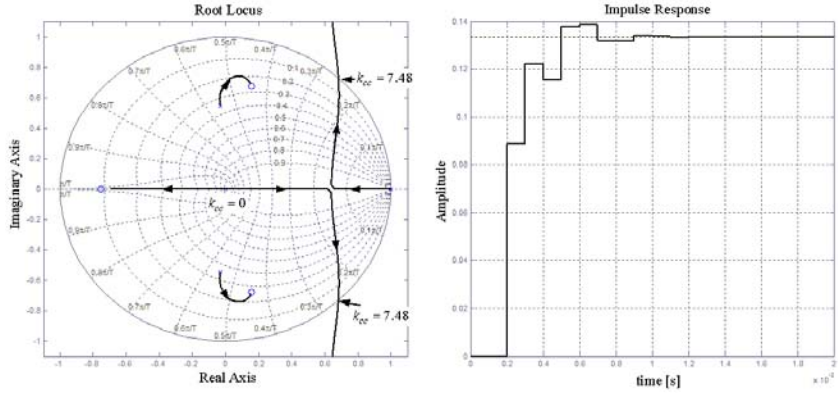
Table 3 shows a summary of the stability margin and dynamic response of the converter-side current tracking scheme, where the results obtained under the nominal system parameters and parameter variation scenarios are presented. It should be pointed out that the stability margins obtained from the converter-side current tracking control scheme are generally higher than those obtained from the grid-side current tracking scheme. However, the converter-side current tracking control scheme is rather sensitive to the variation of the damping resistance. Moreover, if the converter-side current tracking scheme is adopted, then the generation of the reference current would be rather complex since the impedance transfer function between the grid-side and converter-side current must be utilized (see Fig. 1), which would impose additional parameter uncertainty on the control system and complicate the problem. Therefore, the grid-side current tracking control is practically implemented, as reported in the simulation and experimental sections.


Root Locus
Imaginary Axis
Real Axis
$k_{cc} = 9.91$
$k_{cc} = 0$
$k_{cc} = 9.91$
Impulse Response
Amplitude
time [s]

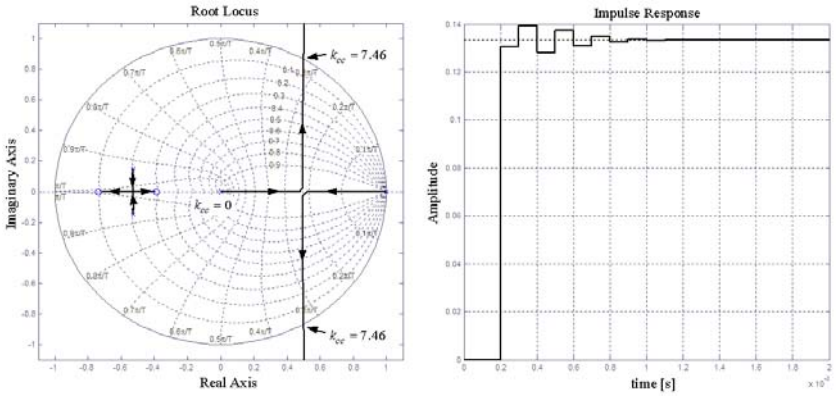
(a)


Root Locus
Imaginary Axis
Real Axis
$k_{cc} = 8.79$
$k_{cc} = 0$
$k_{cc} = 8.79$
Impulse Response
Amplitude
time [s]

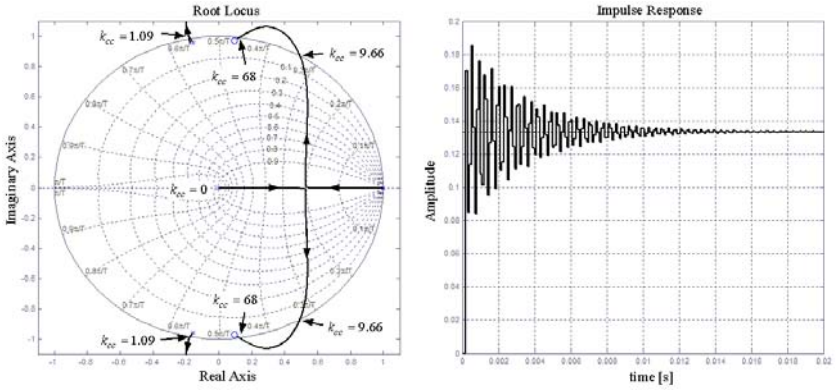
(b)


Root Locus
Imaginary Axis
Real Axis
$k_{cc} = 7.48$
$k_{cc} = 0$
$k_{cc} = 7.48$
Impulse Response
Amplitude
time [s]

(c)



(d)



(e)

Figure 6

The closed-loop root locus diagrams and the open-loop impulse responses of the current regulation algorithm based on the converter-side current (i_c) tracking control scheme. (a) Root locus and impulse response under nominal parameters; (b) Root locus and impulse response under inductance variations; (c) Root locus and impulse response under different control delay (T_d=1.5T_s); (d). Root locus and impulse response under different *RC*-filter capacitance C_d; (e). Root locus and impulse response under different *RC*-filter resistance R_d

In the previous subsections, the closed-loop current tracking scheme was analyzed using root locus methodologies, and the grid-side current tracking scheme and the converter-side current tracking scheme are presented based on the mathematical model of the *LCL*-filter section. It can be noticed that the effect of the AC-side capacitor C_{ac} was not taken into account. Therefore, the effect of the AC-side capacitor will be presented in the forthcoming subsection, where this effect is compensated in the feed-forward loop.

Table 3
Summary of the stability margin and dynamic response of the converter-side current tracking scheme

Case	Marginal gain (deg)	Overshoot (pu)	Response time (ms)
1	9.91	0.155	1.2
2	8.79	0.18	1.4
3	7.48	0.138	1.2
4	7.46	0.14	1.1
5	1.09	0.185	18

3.2.4 Feed-Forward Loop for Load Disturbance Rejection

As is well known, the phase angle of the voltage drop across a capacitor is always a 90-degree lag of the current flowing into the capacitor, which is the basis for the forthcoming derivations. The APF compensating current can be denoted by using the grid-side current of the *LCL*-filter section:

$$\begin{aligned} i_{ga}(t) &= \sum_{n=1}^{N} I_{ga,n} \sin(n\omega_0 t + \varphi_{ga,n}) \\ &= I_{ga,1} \cos(\varphi_{ga,1} - \varphi_{PLL}) \sin(\omega_0 t + \varphi_{PLL}) + I_{ga,1} \sin(\varphi_{ga,1} - \varphi_{PLL}) \cos(\omega_0 t + \varphi_{PLL}) + \\ &\sum_{n=3}^{N} [I_{ga,n}.\cos\varphi_{ga,n} \sin(n\omega_0 t) + I_{ga,n}.\sin\varphi_{ga,n} \cos(n\omega_0 t)] \end{aligned} \tag{44}$$

where N represents the number of the highest harmonic component compensated by the APF. The voltage drop across the AC-side capacitor C_{ac} is represented as:

$$v_{Cac}(t) = \sum_{n=1}^{N} \frac{I_{ga,n}}{n\omega_0 C_{ac}} \sin(n\omega_0 t + \varphi_{ga,n} - \frac{\pi}{2}) \tag{45}$$

the feed-forward loop for the proposed APF can be easily derived by selecting the non-active component of the load current as the reference current in the feed-forward loop, which is represented as:

$$i_{ga,ff}^{ref}(t) = -\{b_{La,1} \cos(\omega_0 t + \varphi_{PLL}) + \sum_{n=3}^{N} [a_{La,n} \sin(n\omega_0 t) + b_{La,n} \cos(n\omega_0 t)]\} \tag{46}$$

Under this scenario, i.e., the non-active component of load-side current is utilized as the feed-forward current (note that the direction should be negative according to the positive direction of APF current defined in Fig. 1) besides, the active current of the VSI generated by the dc-voltage control loop would also have a voltage drop across the capacitor C_{ac}, then the virtual voltage drop across the AC-side capacitor C_{ac} can be denoted as:

$$v_{Cac,ff}^{ref}(t) = -\frac{1}{\omega_0 C_{ac}}(b_{La,1}\sin(\omega_0 t + \varphi_{PLL}) + \Delta I_p \cos(\omega_0 t + \varphi_{PLL})) - \sum_{n=3}^{N}\frac{1}{n\omega_0 C_{ac}}[b_{La,n}\sin(n\omega_0 t) - a_{La,n}\cos(n\omega_0 t)] \quad (47)$$

Hence the feed-forward control signal is obtained as:

$$t_d^{ff}[k] = \frac{\{v_{dc}[k] + v_{grid}[k] - v_{Cac,ff}^{ref}[k]\}T_s}{2v_{dc}[k]} \quad (48)$$

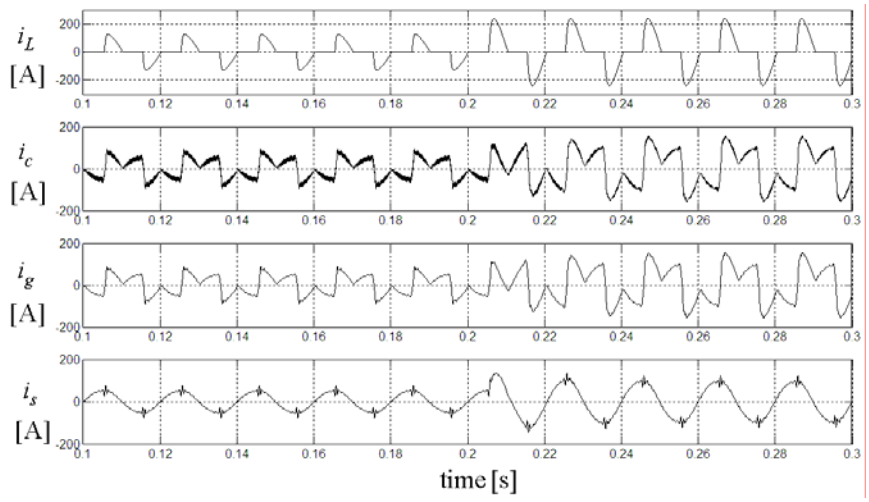
After the feed-forward signal is derived, Eq. (48) can be substituted into Eq. (25) to synthesize the total control signal.

3.3 Dc-Link Voltage Control

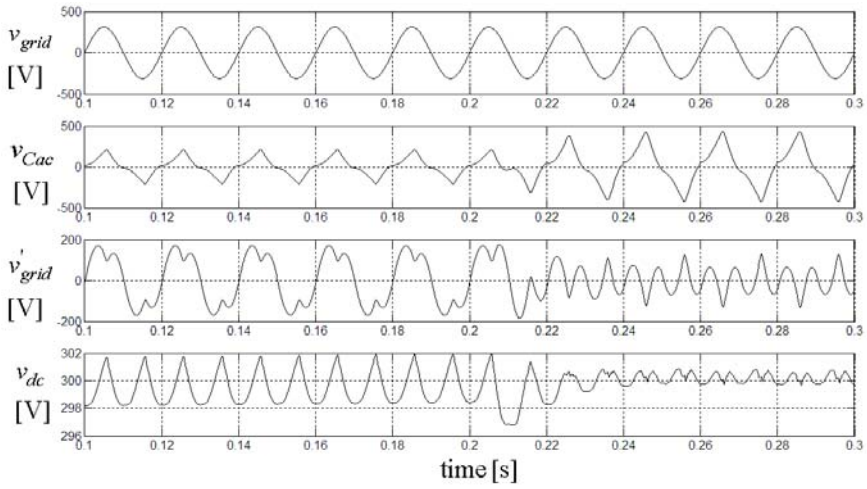
In order to ensure a smooth operation of the APF, the dc-link voltage is sensed by using a potential transducer (PT) and sent to the controller through the A/D channel, where the resetting filter is utilized as a pre-filter for the sampled dc-link voltage. The difference between the dc-link voltage and its reference is regulated by using a proportional-integral (PI) controller (k_i=0.1, k_p=0.6), and the output of the PI regulator is multiplied by a unit sinusoidal function synchronized to grid voltage by using a phase-locked-loop (PLL). The output of the dc-bus voltage regulator is set as the active current reference for the inner current loop (Fig. 3) and also utilized in the feed-forward loop. In addition, to ensure a smooth transient response in the dc-bus voltage, two limiters are used in the control loop, one at the output of the integrator and another at the output of the PI regulator.

4 Simulation Results and Discussions

This section presents the simulation results of the proposed hybrid APF under various parameter variations, including the grid voltage distortion, inductance variations and grid disturbance scenarios. The nominal parameters of the system are listed in Table 1. The thyristor rectifier load is used as a harmonic source, which consists of two anti-parallel connected thyristor switches with resistive load of 2.2 Ω. In order to test the dynamic performance of the presented system, a step change of load is applied by parallel connecting another 2.2 Ω resistor at the load-side of the thyristor switches. Fig. 7 shows the simulation results of the APF under ideal grid voltage and nominal inductances. Fig. 7*a* shows the load current i_L, the converter-side and grid-side currents of the hybrid APF (denoted by i_c and i_g), and the source-side current of the distribution system i_s.



(a)



(b)

Figure 7

The simulation results of the hybrid *LCL*-filter based APF under ideal grid voltage and nominal inductances. (a) The load current i_L, the converter-side and grid-side currents of the hybrid APF (denoted by i_c and i_g), and the source-side current of the distribution system i_s. (b) The grid voltage v_{grid}, the AC capacitor voltage v_{Cac}, the voltage behind the AC capacitor v'_{grid}, and the dc-link voltage of the voltage source inverter v_{dc}

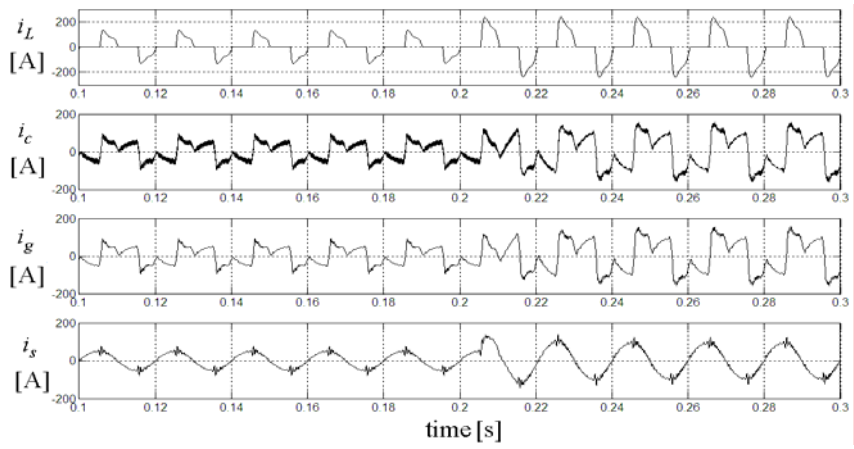
It can be observed that the nonlinear load current i_L, generated by the thyristor rectifier, is highly distorted with sharp rising and falling edges, i.e., a high *di*/*dt* ratio. This kind of load is rather difficult to compensate due to high *di*/*dt* ratio, which requires the compensating device to have sufficient bandwidth to cover the spectrum of the load harmonics. In case of the full compensation scheme, as reported in many previous literature sources [6, 9-12], if the APF were designed to compensate all the non-active component of the load-side current, this would result in ineffective compensation due to the limited current loop gain adopted to ensure the closed-loop stability. If the designer were to aim to improve the compensation performance of the total compensation scheme by increasing the current-loop gain, the system would be prone to be destabilized in the case of compensating a high *di*/*dt* ratio load with sharp rising and falling edges, such as the thyristor rectifier with resistive load considered herein.

Fig. 7*a* shows that the source-side current of the distribution system is sinusoidal and almost in phase with the grid voltage, and the sharp rising and falling edges of load current is well compensated. In addition, the dynamic response of the source-side current is also sufficiently fast when a sudden increase of load is applied at t=0.2s. The converter-side and grid-side currents of the APF (i_c and i_g) can also be observed in Fig. 7*a*, which shows that the high frequency switching ripples in the converter-side current i_c is filtered out by the *RC*-filter hence the injection current i_g is almost ripple free. Fig. 7*b* shows the grid voltage at the common coupling point (PCC), AC capacitor voltage, the voltage behind the AC capacitor (or the virtual grid voltage), and the dc-link voltage of the VSI, denoted by v_{grid}, v_{Cac}, v'_{grid} and v_{dc}, respectively. It shows that the capacitor voltage v_{Cac} and the virtual grid voltage v'_{grid} are highly distorted due to the nonlinear compensating current generated by the VSI.

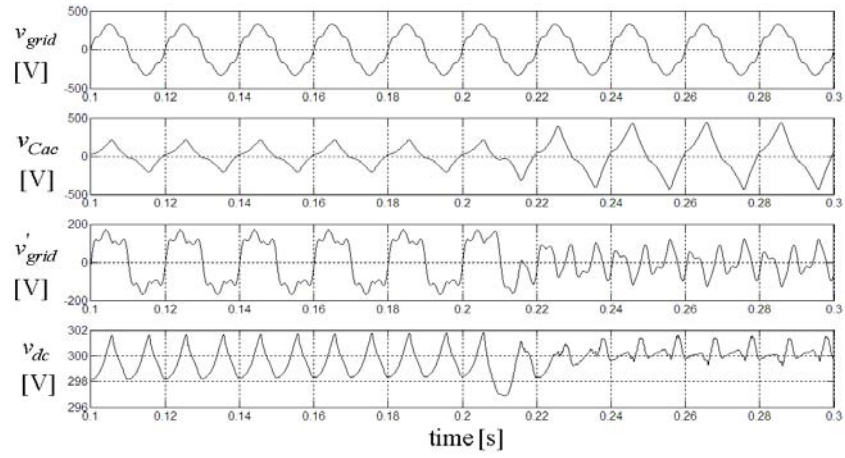
Additionally, it is interesting to notice that the capacitor voltage v_{Cac} undergoes a step increase when the transient increase of load is applied, while the virtual grid voltage, denoted by v'_{grid}, undergoes a decrease of amplitude. Moreover, voltage fluctuation in the dc-link voltage decreases from 4V to 1V when a sudden increase of load is applied. This phenomenon is fundamentally different from the conventional APF with *L*-filter or *LCL*-filter as interfacing inductance [27], where the dc-link voltage fluctuation would increase when a step load increase is applied. In the present case, the reduced dc-link fluctuation is mainly due to the reduction of the virtual grid voltage v'_{grid} after a step increase of load is applied, which shows that the dc-link voltage regulation works more effectively under heavy load for the proposed system.

Fig. 8 shows the simulation results of the proposed hybrid APF under non-ideal grid voltage and inductance variation scenario. It shows that the performance is almost same as in the case of the nominal inductance. However, the only

difference can be observed from Fig. 8*a*, where the source-side current i_s shows a little oscillation at the rising and falling edges of the nonlinear load current. This phenomenon, as stated previously, can be easily attenuated by reducing the current-loop gain. In addition, Fig. 8*b* shows that the grid voltage, AC capacitor voltage, voltage behind the AC capacitor, and dc-link voltage of the VSI are almost the same as in the case under nominal inductance scenario.



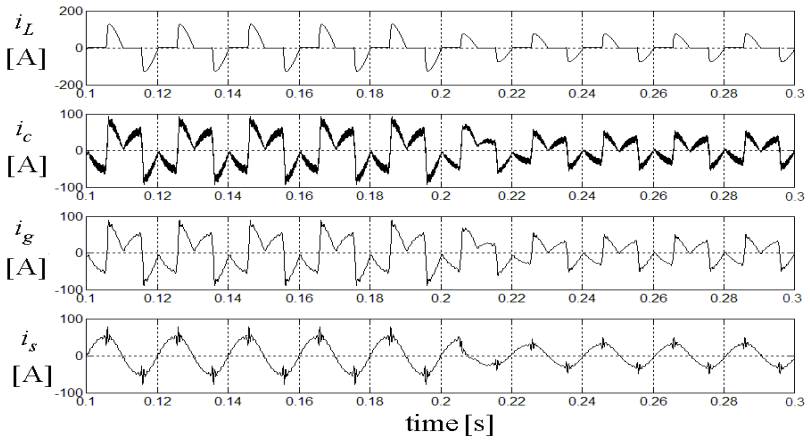
(a)



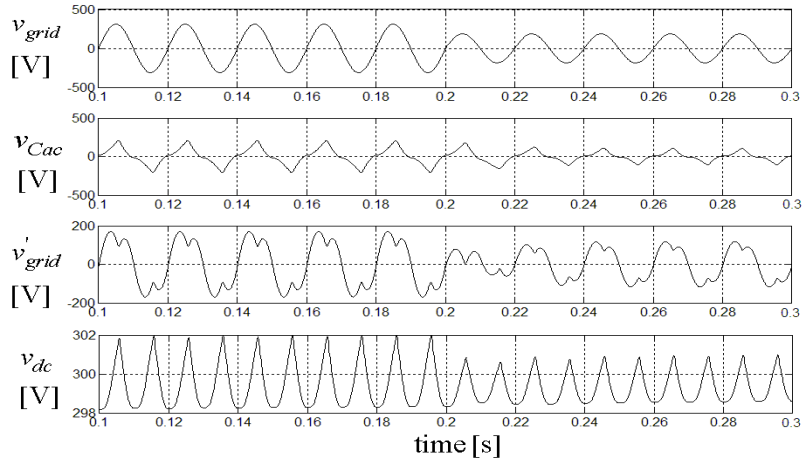
(b)

Figure 8

The simulation results of the hybrid *LCL*-filter based APF under non-ideal grid voltage and inductance variations. (a) The load current i_L, the converter-side and grid-side currents of the hybrid APF (denoted by i_c and i_g), and the source-side current of the distribution system i_s. (b) The grid voltage v_{grid}, the AC capacitor voltage v_{Cac}, the voltage behind the AC capacitor v'_{grid}, and the dc-link voltage of the voltage source inverter v_{dc}



(a)



(b)

Figure 9

The simulation results of the hybrid *LCL*-filter based APF under voltage sag. (a) The load current i_L, the converter-side and grid-side currents of the hybrid APF (denoted by i_c and i_g), and the source-side current of the distribution system i_s. (b) The grid voltage v_{grid}, the AC capacitor voltage v_{Cac}, the voltage behind the AC capacitor v'_{grid}, and the dc-link voltage of the voltage source inverter v_{dc}

Fig. 9 shows the performance of the proposed APF under voltage sag of 0.4 p.u; it shows that the load current reduces significantly when the voltage sag occurs at t=0.2 s. Consequently, the compensating current, either the converter-side current i_c or the grid-side current i_g of the *LCL*-filter section, also undergoes remarkable reduction in magnitude. Further, it can be observed from Fig. 9*a* that the source-

side current shows a satisfactory result with excellent sinusoidal wave shape, with a transient response of less than one fundamental cycle. Fig. 9*b* also shows that the AC capacitor voltage v_{Cac} undergoes a reduction in magnitude when voltage sag occurs, and lower voltage ripple is achieved at the dc-link of the VSI due to the reduction in the compensating current. It can be concluded from the simulation results that a stable operation of the proposed APF is achieved with excellent steady state and dynamic response under parameter variations and grid perturbations, which validates the robustness and effectiveness of the proposed hybrid APF and its control strategies.

5 Experimental Results

In order to further verify the performance of the proposed APF, a hardware prototype system was built in the laboratory using three single-phase VSI topologies. Fig. 10 shows the software architectures of the devised control scheme for the proposed hybrid *LCL*-filter based APF. Three digital signal processors from Texas Instrument[1] (TMS3202812) are adopted in the prototype system. The main controller is responsible for execution of main program, soft-start routine, and protection routine. The auxiliary controller is used specifically for ADALINE-based harmonic extraction algorithm. The third DSP is used for man/machine interface, i.e., parameter display and touch board. The field programmable gate array (FPGA) from Altera[2] (EP1C6Q240C8) is used to receive gating signals from main controller and generate PWM signals for the insulated gate bipolar transistors (IGBTs). In addition, the FPGA also serves as the digital I/O to generate trigger signals for the soft-start circuit, the circuit breaker and other protection circuitry. The insulated gate bipolar transistors (IGBTs) from Semikron[3] are adopted as the power electronic switches for the voltage source inverters.

It should be pointed out that commercial fixed point digital signal processors (DSP), such as TI TMS320F2812, show the characteristic of sequential sampling of the input analog signals. This feature, however, may deteriorate the performance for the APF when real time compensation is required. In order to achieve simultaneous sampling of the analog signals, i.e., the synchronous sampling, the field programmable gate array (FPGA) is adopted as the interface for the two DSPs. In other words, the FPGA serves as the bi-directional random access memory (RAM) for the master and slave DSPs. As shown in Fig. 10, the grid voltages, AC capacitor voltages and the dc-link voltages of the three voltage

[1] Trademark—website: www.ti.com
[2] Trademark—website: www.altera.com
[3] Trademark—website: www.semikron.com

source inverters (VSIs) are obtained from the potential transducers (PTs), and the compensating currents of the APF and the source side currents are obtained from the current transducers (CTs). The fifteen channel signals are preprocessed by the proposed resetting filters, and then sampled by the AD8364 microchips and transmitted to the master DSP. The slave DSP is responsible for the harmonic decomposition of the proposed ADALINE estimation scheme for individual phase. Fig. 10 also shows that the third DSP is adopted to control the touch board and display panel. However, the hardware and control algorithm of the touch board is beyond the scope of this paper and hence it will not be discussed further.

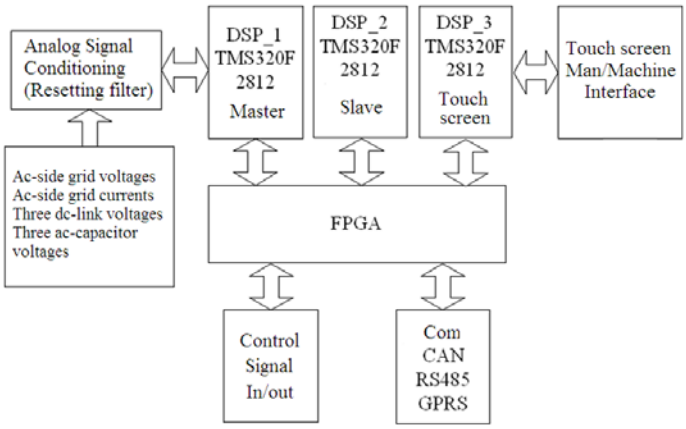
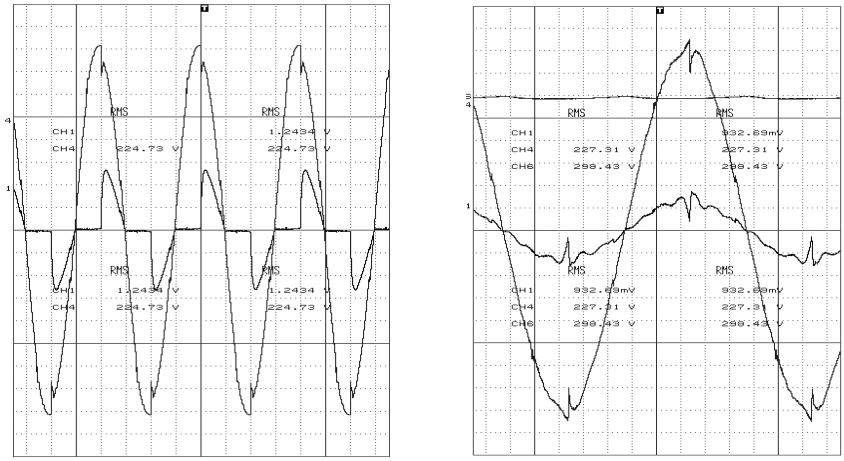


Figure 10
The software architectures of the master/slave digital signal processors and the field programmable gate array for implementation of the proposed control scheme

Fig. 11 shows the steady state experimental results in phase 'A' when the firing angle of the thyristor load is 90 degrees. The total harmonic distortion (THD) of the load current is 75%, which is highly distorted by characteristic harmonics components, such as the 3rd, 5th, 7th and 11th order harmonic components. However, after compensation by the proposed APF, the grid side current shows an excellent sinusoidal waveform, with a distortion of about 13%, which is much less than the load side distortion. In addition, the grid current is almost in phase with the grid voltage, with a power factor of about 0.95. Fig. 11b also shows the waveform of the dc-link voltage, which is consistent with that of the simulation results, with the amplitude of about 300 V.

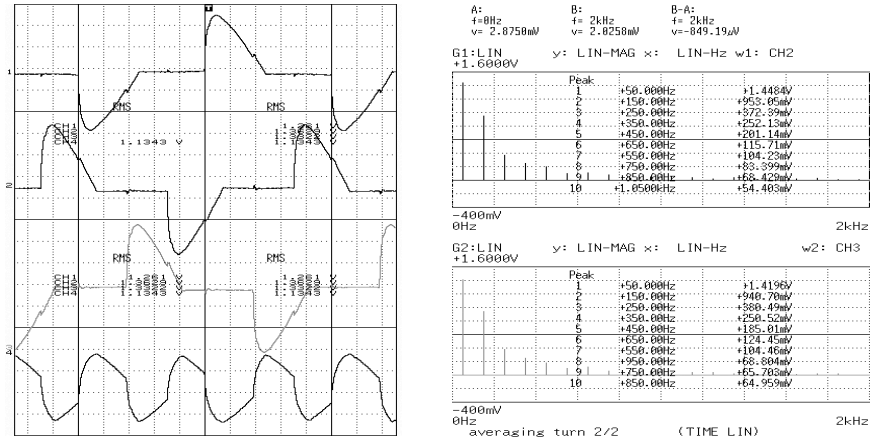


(a) (b)

Figure 11

The experimental results of the APF in phase 'A' with thyristor rectifier load when firing angle=90°. (a) The grid current and voltage (ch-1: 80 A/div, ch-4:40 V/div, X-axis:5 ms/div); (b) The grid current i_{sa} (ch-1: 80 A/div) and the APF dc-link voltage $v_{dc,A}$(ch-3:20 V/div, X-axis:2 ms/div)

Fig.12 shows the load side currents in phase 'A', 'B', 'C', as well as the neutral wire current, and the FFT spectrum of the currents in phase 'B' and 'C'. It can be observed that the load currents are highly distorted and each phase shows a phase shift of 120 degrees. And the neutral wire current is characterized by the 3N (N is integer) order harmonics.

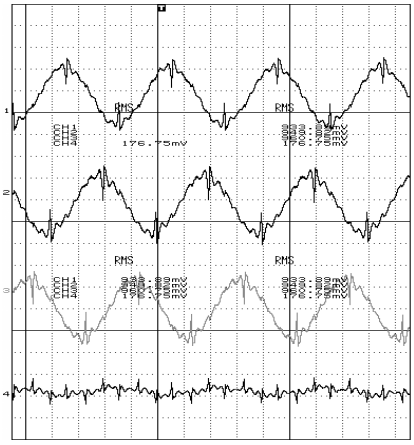


(a) (b)

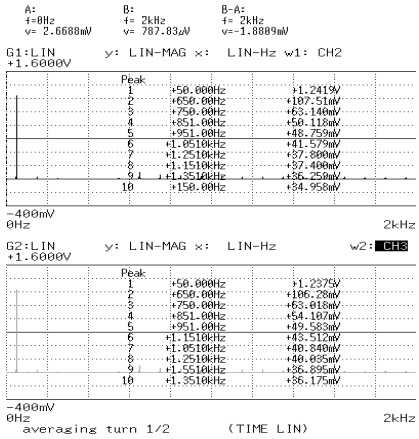
Figure 12

Experimental results of the three single-phase thyristor load when firing angle=90°. (a) The load currents i_{La}, i_{Lb}, i_{Lc}, i_{LN} (ch-1 to ch-4: 80A/div, X-axis: 2ms/div); (b) The FFT spectrum of i_{Lb}, i_{Lc}

After the APF is switched on, it can be observed from Fig. 13 that the grid side currents are almost sinusoidal. In addition, the neural wire current is also well compensated and the 3 N (N is integer) order harmonics are almost eliminated.



(a)



(b)

Figure 13

Experimental results of the grid currents after compensation when firing angle=90°. (a) The load currents i_{sa}, i_{sb}, i_{sc}, i_{sN} (ch-1 to ch-4: 80 A/div, X-axis: 5 ms/div); (b) The FFT spectrum of i_{sb}, i_{sc}

The experimental results illustrated by Figs. 11-13 indicate that the proposed hybrid APF is quite effective for compensating the nonlinear load current with sharp rising and falling edges. The three single-phase topologies of the hybrid APF provides flexible solutions for harmonic and reactive compensation of the three-phase balanced or unbalanced nonlinear load. The consistency between the simulation and experimental results verifies the effectiveness and robustness of the proposed control scheme.

Conclusions

This paper proposes a new APF topology, using the single-phase hybrid *LCL*-filter as the building block. The proposed hybrid APF shows the advantage of the conventional hybrid APF in the sense that the dc-link voltage of the voltage source inverter is significantly reduced compared to the pure APF based on the *L*-filter or *LCL*-filter as the interfacing impedance between the inverter and the grid.

The mathematical modeling of the hybrid APF is presented by using state-space representations. The feed-forward and feedback control scheme is proposed to ensure precise steady-state and dynamic performance of the APF. To reduce the controller bandwidth, the selective harmonic compensation scheme is adopted by using the well-known adaptive linear neural networks. Therefore, the interested harmonics are selected to be compensated to limit the controller bandwidth, thus ensuring the stability of the closed-loop current tracking algorithm.

To verify the effectiveness of the proposed APF, extensive simulation results obtained from Matlab/Simulink are provided under parameter variations and grid voltage disturbances. It is demonstrated by the simulation results that satisfactory compensation is achieved by using the proposed ADALINE-based feed-forward and feedback control strategies. A laboratory prototype system is also built. The digital signal processors (DSPs) and field programmable gate array (FPGA) are utilized as the main controller to implement the control strategies. The feasibility and effectiveness of the proposed APF is substantially confirmed by digital simulation and experimental results obtained from the laboratory prototype system.

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