Enhancing the Measurement of Non-Harmonic Power, using Distributed Microcontrollers

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Abstract: *The current trend of increasing digitalization, places demands on high speed and accuracy of conversion of various analog signals, into their digital form. One example is the need for accurate measurement of power and efficiency in power semiconductor converters operating at switching frequencies up to 100 kHz. A fast four-channel digital oscilloscope is usually used for such purposes; however, it represents a relatively expensive solution. This article describes the possibility of hardware implementation of a significantly more economical measurement system based on distributed architecture and parallel cooperation of multiple microcontrollers, using their implemented analog-to-digital (AD) converters. The proposed approach is based on the time-interleaving technique to overcome the internal limitations of the sampling rate of individual ADC units integrated with the microcontroller, which allows significantly higher effective sampling rates without the need for specialized high-speed external converters. The lowest level of the proposed architecture consists of several microcontrollers operating in parallel, each performing periodic sampling, with well-defined phase shifts, with respect to a common reference clock signal. To ensure deterministic timing behavior in all acquisition channels, a central synchronization mechanism consisting of a master microcontroller is designed. Special emphasis is placed on the clock distribution strategy, trigger signal integrity, and latency minimization in order to achieve subsample alignment accuracy. Experimental verification is performed on a prototype system, composed of multiple synchronized microcontroller units. The results confirm that the interleaved architecture achieves an almost linear increase in the effective sampling rate proportional to the number of parallel channels, while maintaining acceptable accuracy and stability.*

Keywords: measurement, A/D conversion, interleaved mode, microcontroller, distributed system

1 Introduction

The increasing demand for high-speed data acquisition in modern electronic systems has intensified the need for efficient analog-to-digital conversion techniques, that can overcome the limitations of single-channel architectures.

Applications such as software-defined radio, industrial diagnostics, and embedded sensing require sampling rates that often exceed the capabilities of standard microcontroller-integrated ADCs. Time-interleaved ADC (TI-ADC) architectures represent a proven solution that enables higher effective sampling rates by operating multiple converters in parallel with phase-shifted clocks [1-7]. Recent works demonstrates multi-GS/s performance using interleaving in combination with advanced calibration and digital correction techniques [8-12].

Current research has focused on mitigating the fundamental limitations of TI-ADC systems, particularly channel mismatch errors such as offset, gain, and timing distortion. These imperfections significantly degrade dynamic performance metrics including SNDR and SFDR [13-16]. State-of-the-art approaches use digital background calibration, machine learning, and adaptive synchronization techniques to address these challenges [17-20]. Notably, modern calibration frameworks based on neural networks or synchronization models have demonstrated substantial improvements in accuracy and robustness under various operating conditions [21].

Along with advances in integrated ADC design, interest in distributed and modular data acquisition systems is growing. Instead of monolithic IC implementations, multiple low-cost microcontrollers can be used to emulate the behavior of the TI-ADC. STMicroelectronics' NUCLEO development boards, with their 12-bit ADC, DMA support, and advanced timer synchronization capabilities, provide a suitable platform for such implementations. By coordinating multiple units using shared triggers and precise timing control, it is possible to create an interleaved ADC system, extending the effective sampling rate beyond the limits of a single device [22-27].

However, implementing interleaving across multiple devices introduces additional challenges compared to integrated solutions. These include synchronization across distributed clock domains, communication latency, and increased timing uncertainty. Even small timing discrepancies can significantly degrade system performance, requiring precise clock alignment and trigger distribution [28].

Furthermore, the scalability of such systems is limited by cumulative misalignment errors and data transfer limitations. While increasing the number of interleaved channels improves sampling throughput, it also amplifies the impact of non-idealities and increases calibration complexity. Recent studies emphasize that an efficient system design must combine hardware synchronization, efficient data acquisition (e.g., DMA-based sampling), and digital post-processing techniques to achieve acceptable performance [8][19].

This paper investigates the feasibility of implementing a distributed TI-ADC system using multiple NUCLEO development boards. These boards integrate an ST-Link debugger/programmer, which is essential for uploading firmware to the microcontroller memory. Using these boards, it is possible to design a microcontroller-based system architecture capable of digitally measuring the input power, output power, and consequently the efficiency of devices whose signals

operate at frequencies up to 100 kHz [29][30]. The proposed approach aims to demonstrate that a network of embedded microcontrollers can provide a flexible and cost-effective alternative to conventional high-speed ADC architectures while maintaining acceptable accuracy for practical applications.

2 Selection of Development Boards and Microcontroller

STMicroelectronics offers three NUCLEO three types of boards: NUCLEO-32, NUCLEO-64, and NUCLEO-144 with variants grouped by supply voltage and performance [31]. The primary distinguishing factor among these groups is the integrated microcontroller. Depending on the variant, the microcontroller is designed for general-purpose use, high performance, or low power. Figure 1 shows the distribution of NUCLEO boards by type and memory size.

	Nucleo-32	**Nucleo-64**	**Nucleo-144**
2MB			Nucleo-L4R5ZI Nucleo-L4R5ZI-P Nucleo-H755ZI-Q Nucleo-H753ZI Nucleo-H745ZI-Q Nucleo-F439ZI Nucleo-H743ZI Nucleo-F429ZI Nucleo-F767ZI
1MB		Nucleo-L476RG	Nucleo-L4A6ZG Nucleo-L496ZG Nucleo-L496ZG-P Nucleo-F756ZG Nucleo-F746ZG Nucleo-F413ZH Nucleo-F207ZG Nucleo-F412ZG
512kB		Nucleo-L452RE Nucleo-L452RE-P Nucleo-F446RE Nucleo-F411RE Nucleo-G474RE Nucleo-F401RE Nucleo-F303RE Nucleo-L4152RE	Nucleo-F303ZE Nucleo-F722ZE Nucleo-F446ZE
256kB	Nucleo-L432KC	Nucleo-F091RC Nucleo-L433RC-P	
192kB		Nucleo-L073RZ	
128kB	Nucleo-L412KB Nucleo-G431KB	Nucleo-L412RB-P Nucleo-F410RB Nucleo-G431RB Nucleo-G070RB Nucleo-G071RB Nucleo-F070RB Nucleo-F072RB Nucleo-F103RB Nucleo-L010RB	
64kB	Nucleo-F303K8 Nucleo-F301K8	Nucleo-F334R8 Nucleo-L053R8 Nucleo-F030R8 Nucleo-F302R8	
32kB	Nucleo-F031K6 Nucleo-F042K6 Nucleo-F301K6		
16kB	Nucleo-L011K4		

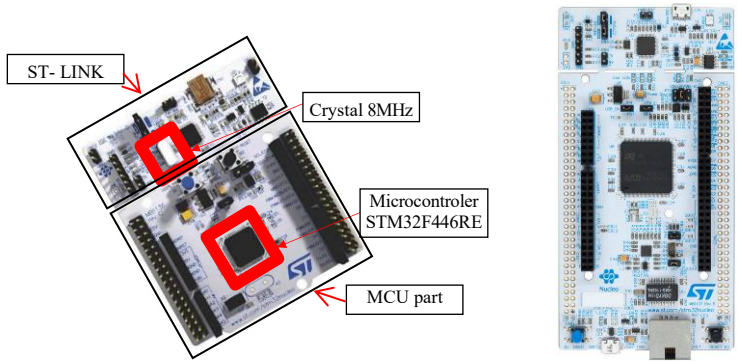
Figure 1

Flash memory size for individual types of Nucleo boards:

Mainstream, Ultra low-power, High performance

Selecting a NUCLEO-64 board offers an optimal compromise, including DSP-enabled microcontrollers (F7, F4, F3, L4) with mid-range memory and varying

performance levels. For example, the NUCLEO-L053R8 operates at 32 MHz, while the STM32F446RE microcontroller on the NUCLEO-F446RE reaches 180 MHz, making it suitable for high-speed A/D conversion. For the control unit, the NUCLEO-F746ZG with the STM32F746ZG microcontroller was selected.



(a) (b)

Figure 2
(a) NUCLEO-F446RE development board, (b) NUCLEO-F746ZG development board

3 Design of a Four-Channel A/D Conversion System

The selected STM32F746ZG microcontroller and STM32F446RE microcontroller serve as the system's main hardware. Measuring input and output power requires four signals (voltage and current), so the system must include four conversion channels [32][33].

Each STM32F7 and STM32F4 microcontroller has three 12-bit A/D converters operating up to 45 MHz, with a simultaneous mode that samples three signals at once [34][35]. However, this is insufficient for four signals. Additionally, for a 100 kHz signal with a 333.33 ns sampling time (15 ADCCLK cycles), only 30 samples per period are obtained [36]:

$$N_{vzoriek} = \frac{f_{ADC}}{f \cdot smp} = \frac{45 \cdot 10^6}{100 \cdot 10^3 \cdot 15} = 30 \tag{1}$$

where f_{ADC} is the A/D converter frequency, f is the frequency of the input signal being converted, and smp represents the number of clock cycles required for a single A/D conversion (smp equals 15 ADCCLK cycles in this case).

In interleaved mode, a 100 kHz signal yields three times more samples than a single A/D converter, increasing from 30 to 90 samples per period and improving accuracy, though it may still be insufficient.

Since the selected microcontrollers cannot provide higher sampling rates, the solution is either more expensive faster A/D converters or using additional STM32F446RE microcontroller units. The proposed design uses three per channel, achieving up to 27 Msps and about 270 samples per period of a 100 kHz signal. The main challenge is precise synchronization and timing of the A/D converters.

Figure 3 shows the system's block diagram:

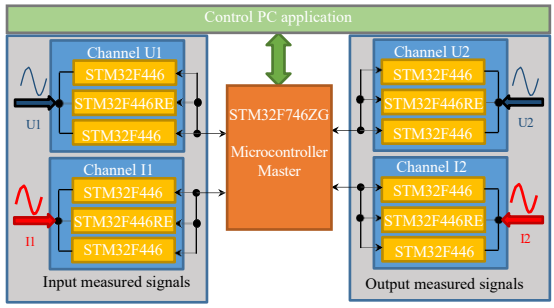


Figure 3

Design of a distributed measurement system with STM32 microcontrollers

3.1 Clock Synchronization Setup between Microcontrollers

The use of multiple microcontrollers requires precise synchronization to ensure correct system operation and measurement accuracy.

All used boards (NUCLEO-144 with the STM32F746ZG microcontroller as Master and NUCLEO-64 with STM32F446RE microcontroller as Slaves) include 8 MHz crystals, which could be used for synchronization. However, measurements showed (Fig. 4) that crystal frequency deviations significantly affect performance and accuracy, making this approach unsuitable.

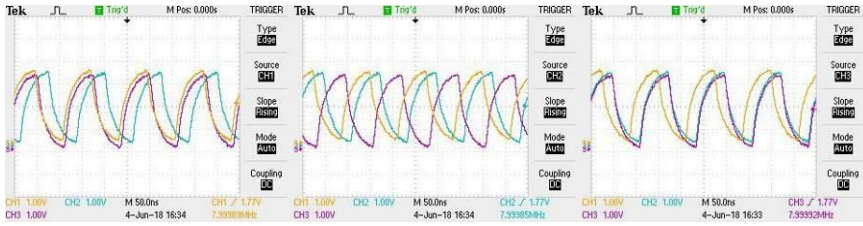


Figure 4

Frequencies of three microcontrollers with independent clock sources

Based on the measured results, the Master microcontroller (STM32F746ZG microcontroller) is driven by an 8 MHz crystal and uses the MCO function to output a clock signal for synchronization. The Slave microcontrollers (STM32F446RE microcontroller) have their crystals disconnected and are synchronized via equal-

length coaxial cables, connecting the Master's PC9 pin to the Slaves' PH0 pins (Fig. 5).

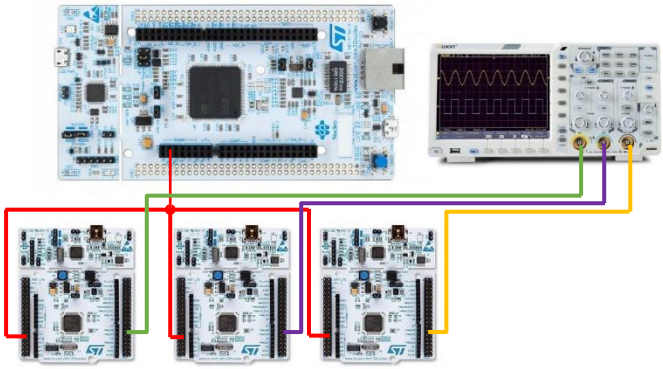


Figure 5
Clock synchronization between Master STM32F746ZG and three Slave STM32F446RE microcontrollers

The measured results for this configuration are shown in Fig. 6. The identical measured frequency of 7.99994 MHz is sufficient to achieve the required synchronization.

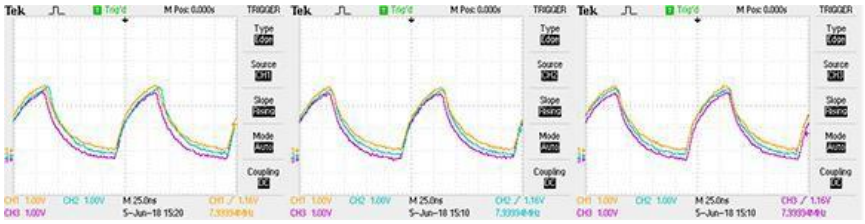


Figure 6
Frequencies of microcontrollers synchronized from a single clock source

3.2 Design of a Distributed Interleaved Mode for A/D Converters

The conversion accuracy of the system depends on several factors, one of which is the sampling density of the acquired signal, where precisely defined time intervals between samples must be maintained. Since further increasing the sampling frequency of the STM32F446RE microcontroller is not feasible, a Distributed Interleaved Mode (DIM) has been proposed, consisting of two components. The first component is the interleaved mode implemented by the STM32 microcontroller manufacturers. The second component is the interleaved mode implemented across multiple STM32F446RE microcontrollers (DIM).

The principle of DIM involves triggering the converters on individual microcontrollers at precisely defined time intervals. When using only the interleaved mode, it is necessary to respect the minimum prescribed delays for triggering ADC2 and ADC3. This delay requirement applies solely within a single microcontroller. By employing additional microcontrollers, this delay can be effectively reduced. The principle of DIM is illustrated in Fig. 7. The aforementioned rule regarding the precise delay in triggering converters applies only to the sampling phase and not to the conversion phase.

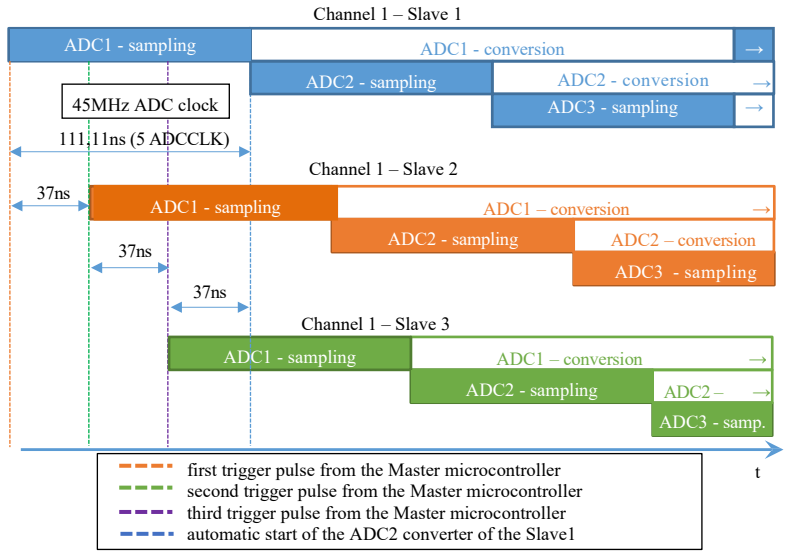


Figure 7

Design of the distributed interleaved mode (DIM)

The figure illustrates the A/D converters of three microcontrollers forming a single channel, labeled as Slave 1, Slave 2, and Slave 3. According to the datasheet, the A/D converters operate at a frequency of 45 MHz. This means that, in the fastest possible mode, the interleaved mode triggers the converters at intervals of 111.11 ns. Using the Distributed Interleaved Mode, it is possible to trigger the ADC1 converters on Slave 2 and Slave 3 microcontrollers with a specific time delay, effectively achieving a threefold increase in the number of samples compared to the standard interleaved mode. The advantage of this approach is higher measurement accuracy; however, it requires greater memory storage capacity.

Based on Fig. 7, a 37ns trigger delay from the Master requires dedicated lines instead of a standard bus. Line lengths must be equal and as short as possible. The STM32F746ZG microcontroller uses pins PF0, PF1, and PF2 to send start signals to the Slave A/D converters. The Master generates start pulses at defined intervals to implement DIM mode, and these lines are connected in parallel to the identical channels.

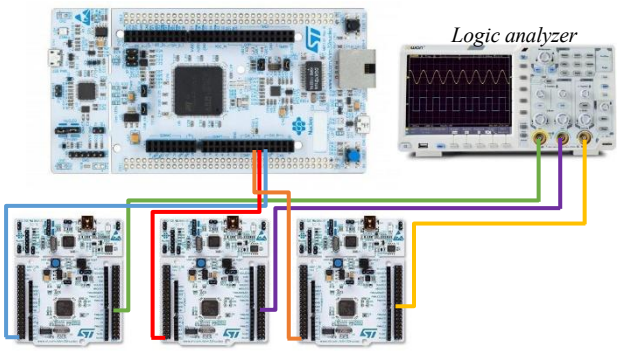


Figure 8
Connection of trigger lines for A/D converters of a single channel

Wiring and functional verification of the device were performed using a Tektronix TLA6202 logic analyzer. The A/D converters provide status bits indicating conversion error, start, and end of conversion. During DIM mode testing, start and end signals were monitored, triggering interrupts that execute specific functions. A logical high (1) is set at the start of conversion and a logical low (0) at the end.

Three lines from each microcontroller (nine total) were connected to the analyzer, with each A/D converter assigned a dedicated line. Results are shown in Fig. 9.

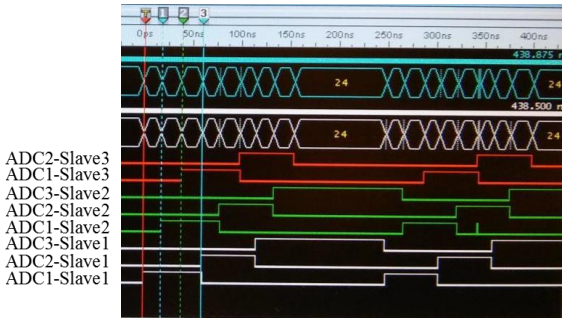


Figure 9
Verification of the DIM mode, corresponding to Fig. 7, using a logic analyzer

3.3 Design of Communication between Master and Slave Microcontrollers

The next step is designing communication between the STM32F746ZG microcontroller and STM32F446RE microcontroller, enabling data exchange between the Master and Slave microcontrollers for coordinated processing.

Given the need for high data rates in a system with 12 Slave microcontrollers, suitable interfaces were evaluated. Although both USART (synchronous) and SPI offer high speeds, USART is limited to 8-bit transfers, which is insufficient for a 12-bit A/D converter. Therefore, SPI (up to 50 Mbit/s) was selected, despite requiring more lines, as each Slave needs a separate SS pin.

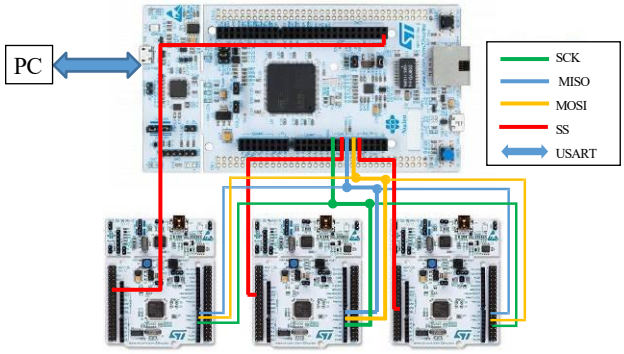


Figure 10
Communication design of a single channel between Master and Slave microcontrollers via SPI interface (connections for other channels are identical)

Communication between the Master microcontroller and the computer is handled via the asynchronous USART interface.

All Slave microcontrollers are reset simultaneously by sending a logical low (0) signal from the Master to their RESET pins. The design also uses optocouplers on all interconnections to ensure galvanic isolation and protect the system.

3.4 Implementation of the Hardware Component of the Multifunctional Measurement System

The complete wiring of the proposed measurement system during the phase of testing its basic functions is shown in Fig. 11.

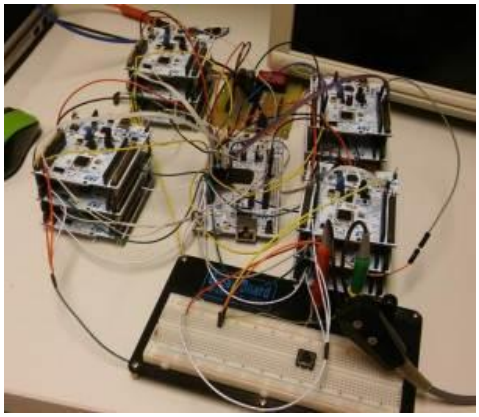


Figure 11
Wiring of the multifunctional measurement system during basic function testing

Along with the hardware, an analog input stage was designed to keep the signal within the 0–3.3 V range of the STM32F446RE microcontroller A/D converters, as they cannot measure voltages above this limit or negative values. The circuit also adds a DC offset to shift the signal into the 0–3.3 V interval.

3.5 Implementation of the Input Analog Section

The analog section (Fig. 12) enables measurement of AC and DC voltages across multiple ranges, providing 1:1 and 1:10 division ratios, as well as selectable scaling factors of ×100, ×20, ×10, ×2, ×1, ×0.5, and ×0.2 [37][38].

Figure 12
Block diagram of the analog section implementation

A 1:1 division allows measuring the original signal at the A/D converter input, while a 1:10 division reduces it tenfold, enabling measurement up to 33V (with zoom ×1).

Input signal zoom provides amplification or attenuation: amplification scales low signals to the reference range, while attenuation (×0.5, ×0.2) corresponds to a 1:10 division. Combining division and zoom allows measuring up to 50V (DC), and a ×10 probe can further increase this range.

The circuit diagram and implementation are shown in Fig. 13 and Fig. 14.

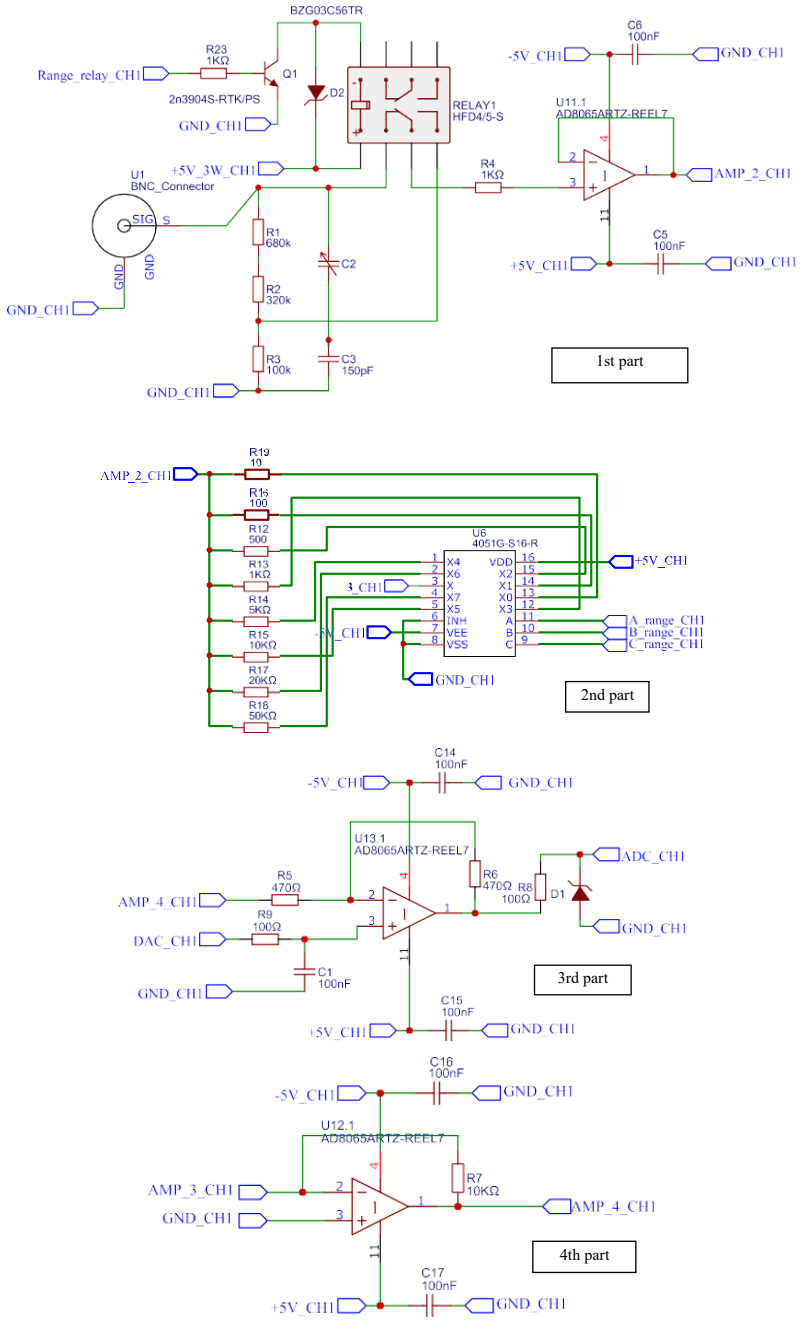


Figure 13
Circuit diagram of the analog section

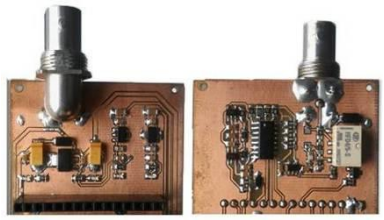


Figure 14
Printed circuit board of the analog section

The analog section consists of four blocks. The first block directs the input from the BNC connector and selects a 1:1 or 1:10 divider via a reed relay controlled by the microcontroller. In 1:1 mode, the signal goes directly to a buffer amplifier; in 1:10 mode, it is attenuated before amplification. The buffer output (AMP_2_CH1) feeds the second block, where a multiplexer selects resistor combinations to set the zoom factor. The third block uses an inverting amplifier to apply gain or attenuation based on the selected resistance and feedback resistor (10 kΩ), and the fourth block inverts the signal and adds a DC offset from a D/A converter to keep it within the 0–3.3 V range for the STM32F446RE microcontroller A/D converter.

3.6 Final Hardware of the Measurement System

Based on achieving the required functionality of the tested configuration of the proposed four-channel measurement system using Nucleo development boards, a final version was also implemented using the same microcontrollers and their interconnection, but based on a custom-designed printed circuit board.

To ensure easy maintenance of the measurement system, a modular design was chosen, with a carrier Master PCB containing the Master microcontroller as the base. Individual Slave microcontrollers (on Slave PCBs) are connected to this board via connectors, as shown in Fig. 15.

Figure 15
Final version of the hardware implementation of the multifunctional measurement system

The power supply and PC communication section is located on the right side of the PCB. In addition to the power connector and USB mini connector, a three-pin header for programming and debugging the microcontroller, a RESET button, and a current fuse are visible. The upper section of the PCB contains two types of

TRACO converters: a TEL 3-1211 isolated TRACO converter with a 5V output, and a TDN 3-1222W isolated TRACO converter with a ±12 V output.

The first TRACO converter powers all the microcontrollers, while the second TRACO converter supplies the operational amplifiers with ±12V. The power supply for the Master microcontroller is provided through a linear voltage regulator, AMS1117-3.3, which stabilizes the voltage at 3.3V. A similar function is performed by the linear voltage regulator KIA1117-5.0, which stabilizes the voltage at 5V. The output of this regulator is used to power the optocouplers. The circuit diagrams of the power supplies are shown in Fig. 16.

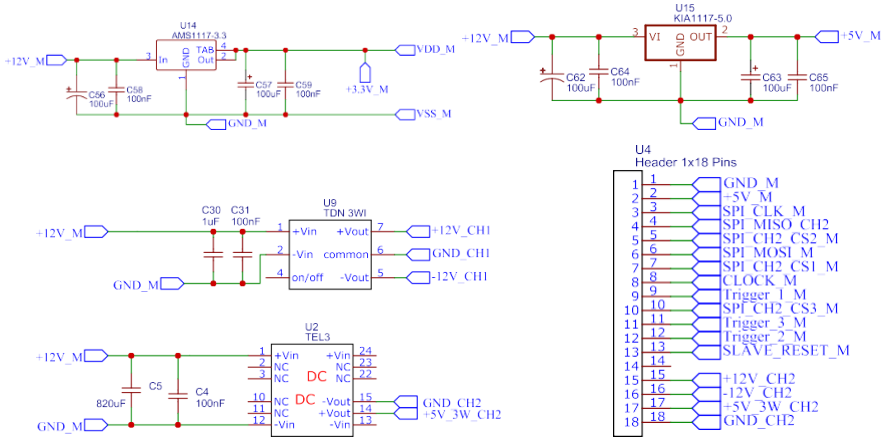


Figure 16

Circuit diagram of TRACO converters, voltage regulators, and connector header

The labels +12V_M and GND_M represent the power supply and ground from the power connector on the Master PCB. The circuit in the upper left serves to stabilize the voltage at 3.3V, which powers the Master microcontroller. A similar circuit is present on the PCB of each channel. The upper right section of the figure shows the circuit responsible for generating a 5V output voltage, which powers the optocouplers.

Another block consists of the TRACO converter power supply circuits, visible on the left side below the voltage regulator circuit. These circuits provide galvanic isolation of the power supply between the Master PCB section and the Slave microcontrollers. The final part of the schematic is the connector header, which connects to the channel PCB. The Master PCB includes four connector headers corresponding to the four channels. All communication, clock, and control pins from the Master microcontroller are routed to these headers.

3.7 Software solution

Due to the complexity of the final software solution, only a simplified flowchart is presented in Fig. 17. Fig. 17(a) shows the communication interface between the PC application and the Master and Slave microcontrollers, while Fig. 17(b) outlines the main operation of the Slave microcontroller. The system includes calibration of the AD converter using the integrated DA converter. Although a single AD converter processes only 2000 samples per cycle, low-frequency and DC measurements are enabled by programmatically reducing the converter clock frequency from 45 MHz to 22.5 MHz, 11.25 MHz, and 5.625 MHz.

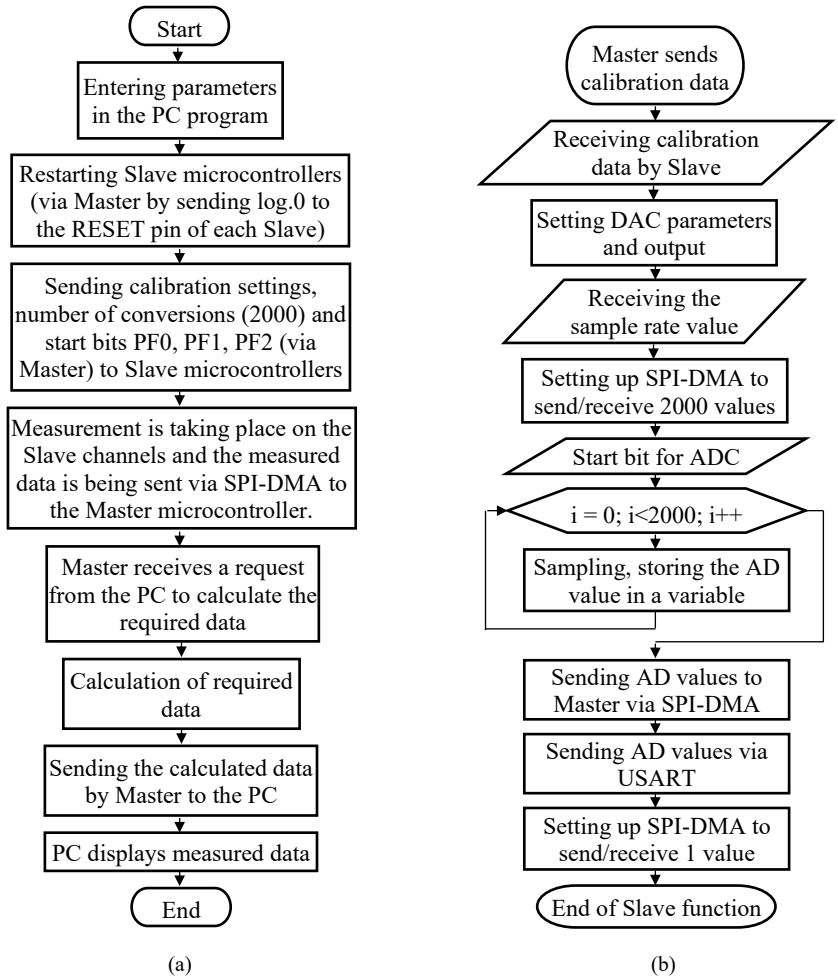


Figure 17
(a) Flowchart of communication between the control application in the PC, the Master and Slave microcontrollers, (b) Flowchart of operations performed by the Slave microcontroller

3.8 Verification Measurement of Non-Harmonic Power

The functionality of the implemented measurement system and the verification of its parameters were performed by measurements on a Buck converter connected as shown in Fig. 18.

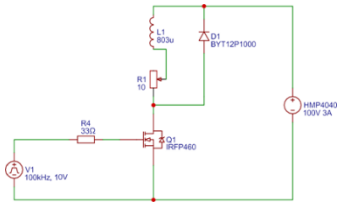


Figure 18
Circuit Diagram of the Measured Converter

During the measurements, an HMP4040 power supply was used, set to 100 V, with the circuit drawing currents of 1.2A and later 2.8A. An Arbitrary Generator HMF2525 was employed to drive the transistor, generating a 100 kHz rectangular signal with a 50% duty cycle and a voltage range of 0–10V. The monitored and measured quantities were the voltage u_{DS} and the current i_D of the MOSFET transistor designated IRFP460, as shown in Fig. 19.

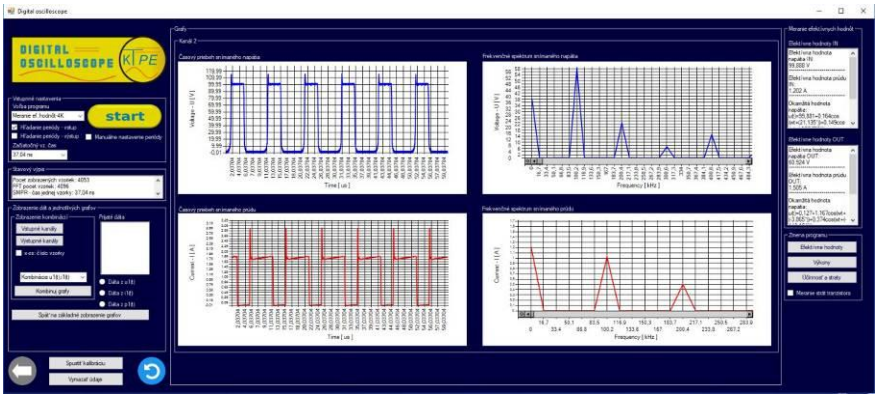


Figure 19
Recorded waveforms of the transistor voltage u_{DS} and current i_D and their frequency spectra

Another performed measurement involved assessing the losses in the transistor. This measurement was conducted at a converter voltage of 100V and a DC source current of 2.8A, with a converter switching frequency of 100 kHz. The results are shown in Fig. 20.

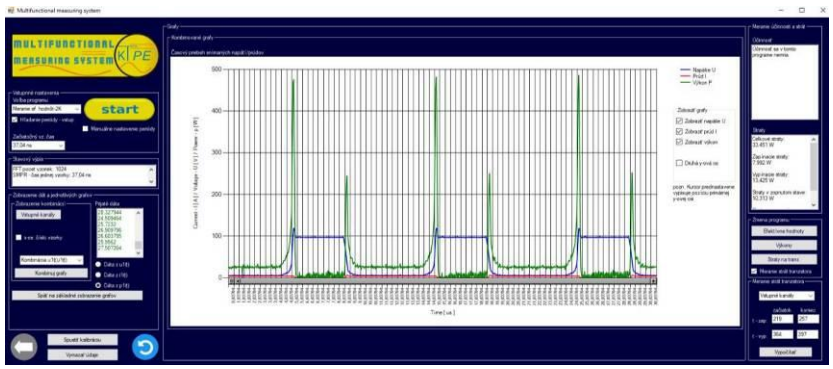


Figure 20
Representation of MOSFET transistor power losses

The measured voltage and current results of the transistor obtained using the constructed measurement system were compared with measurements performed using a Tektronix DPO 7354 oscilloscope. In the following Fig. 21, the percentage deviations of the measured quantities are presented, recorded on two different channels. The measurements were conducted over a frequency range from 100 Hz to 100 kHz.

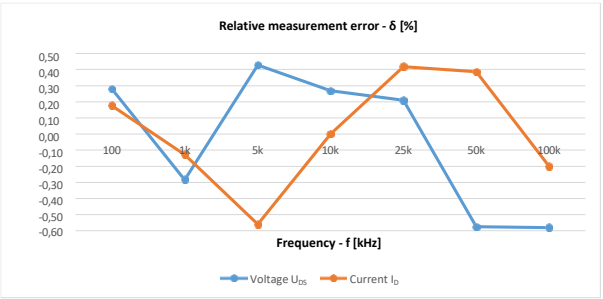


Figure 21
Measurement deviations of voltage and current using the constructed measurement system

The measured data indicate that the maximum deviation of the measurements obtained with the constructed measurement system is approximately ±0.55%.

4 Conclusions

The obtained results confirm the practical feasibility of improving the measurement system's accuracy, by employing a distributed system of microcontrollers. During the implementation, it was determined that the delay time for triggering the converters of individual microcontrollers could be reduced to approximately 7ns

using the Master microcontroller. This implies that the total number of microcontrollers forming the distributed system could be increased to up to 15.

In addition to accommodating a larger number of microcontrollers, it is also possible to use other, more powerful, processor types, such as the STM32G4 microcontroller, which is specifically designed for signal acquisition. These microcontrollers include up to five A/D converters, which could enable even more precise measurements using the distributed configuration described above. The resulting measurement system would thus achieve performance comparable to commercially available systems, but at roughly one-tenth of their cost.

References

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