Comparative Study of PSFB Converter Efficiency for Various GaN Semiconductor Devices

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Abstract: This paper aims to provide a comprehensive understanding of the semiconductor selection process for the inverter of a Phase-Shifted Full-Bridge (PSFB) converter supported by simulation and measurements. We compare three semiconductor technologies, Si, SiC, and GaN, based on their zero-voltage switching (ZVS) capabilities. The output capacitance of the switch highly influences the ZVS range of the converter. Wide band-gap devices have smaller output capacitances and thus, allow the extension of the ZVS range, without additional hardware. This resaerch strengthens the influence of output capacitance fine-tuning on the converter efficiency when selecting the semiconductor switches. The comparison is supported by simulation in the program PLECS for a whole family of GaN transistors. The work herein presents a detailed analysis of the advantages and limitations of each semiconductor technology, thereby providing insights and recommendations for selecting the most suitable semiconductor for high-efficiency PSFB converters. The results are supported by a measurement on the 600 W, 100 kHz laboratory model of the PSFB converter.

Keywords: GaN; high efficiency; phase-shift full-bridge converter; Plecs; semiconductor selection; SiC

1 Introduction

The Phase-Shifted Full-Bridge (PSFB) topology has been popular over the years because it achieves high efficiency, mainly due to the natural zero voltage switching (ZVS) on the primary side. This, with the advantage of galvanic isolation of the primary and secondary sides, wide input and output ranges, and a large conversion ratio, makes it an interesting topology for a highly efficient converter [1].

While the converter concept has been known for decades, the current development of semiconductors [2] has opened up new possibilities. The PSFB converter can now be applied in a wide range of scenarios, from grid-tied photovoltaic

applications [3] to chargers for electric vehicles [4-6], and even in DC grids for renewable systems. Its versatility is further demonstrated in applications such as hybrid vehicles and converters between 48 V and 12 V systems.

In addition to the advantages, PSFB also has disadvantages. ZVS is dependent on the resonant circuit between the leakage inductance of the transformer and the output capacitance (C_{oss}) of the switching transistors. Increasing the frequency, which results in a higher power density of the converter, reduces the transformer's leakage inductance. Therefore, reducing the C_{oss} of the switching transistors is necessary to achieve ZVS for a wide load range. For high-frequency applications, it is also necessary to reduce the gate charge. Modern Gallium Nitride (GaN) and Silicone Carbide (SiC) based semiconductor technologies make this possible [9]. Moreover, GaN technology features zero reverse recovery losses [15] [18]. As an alternative to the ZVS problem, the addition of inductance may be considered rather than a reduction in C_{oss}. However, this approach also has limitations, namely a reduction in the effective phase shift period and the necessity for additional fast diodes that can handle the input voltage and overvoltage oscillation to remove oscillations from the switching transistors [14] [19].

In general, the PSFB converter has the same inverter topology, but the rectifier varies according to the output current and voltage levels. The inverter topology is significant as it determines the overall performance and efficiency of the converter. The most common rectifier topologies are the full bridge rectifier, the center-tapped rectifier, and the current doubler. Each of these rectifiers has its unique advantages and limitations, and the choice of rectifier depends on the specific application requirements. In this case, a current doubler is implemented, which offers the advantage of requiring a transformer with a single winding and the use of two rectifier transistors [20].

This paper delves into the semiconductor selection for the inverter of the PSFB converter, particularly when used with a current doubler rectifier. The proposed converter is designed to operate in combination with a power factor correction (PFC) rectifier, with an input supply voltage of 390 V, an output voltage of 24 V, and a maximum power of 600 W. The inverter operates at a frequency of 100 kHz.

The paper is organized as follows. The first part of the article describes the conditions for achieving ZVS in the PSFB converter, which is widely used because of its ability to achieve high efficiency and high transfer ratio. The second section also highlights the efforts to reduce the capacitive energy in the circuit, a significant part of which is the output capacitance of the transistors. The third section points out that GaN and SiC technology have a multiplicatively smaller capacitance relative to the series resistance, which predestines them for use in a given inverter. The fourth section of the article focuses on the measurement of ZVS achievement and efficiency under laboratory conditions and includes an analysis of the thermal images captured. Section 4 provides a summary and concludes this paper.

2 ZVS Design Consideration

To achieve the necessary ZVS for high efficiency, it is important to meet the sufficient inductive energy and dead time criteria.

To satisfy the inductive energy condition, it is necessary that the circuit, as shown in Fig. 1, contains sufficient inductive energy E_L to overcharge the output capacitances of the transistors according to equation (1) [20] [21]. The capacitors in Fig. 1 represents just the output capacitances of transistors and are not added as separate components. It must be taken into account that the capacitive energy is not only formed by the output capacitance of the transistors but also by parasitic capacitances in the transformer and at the PCB [21]. The capacitive energy is defined by time-related transistor output capacitance $C_{OSS(tr)}$, parasitic capacitance of the transformer C_{XFMR} and the input voltage V_{IN}. This capacitance is listed in the datasheet as C_{OSS}, which reflects the static capacitance measurement of the transistor. Still, the datasheet also lists the value of $Co_{(tr)}$, which is the output capacitance when the voltage drops from a defined value (400 V for the GS-065 transistor) to zero, thus accounting for the dynamic behavior when the capacitance nonlinearity appears from the voltage.

$$E_L \geq 0{,}5(2C_{oss(tr)} + C_{XFMR})V_{IN}^2 \tag{1}$$

The problem is that there is a different amount of inductive energy for the leading and lagging leg, because the recharging occurs at different times as shown in Fig. 2. As the output capacitance of the leading leg transistor is discharged, the primary current reverses its polarity. This results in the current in the rectifier transistors on the secondary side commuting such that the voltage on the secondary side of the transformer is zero. This indicates that the inductive energy available to the leading leg is primarily constituted by the leakage inductance of the transformer, defined by (2). For the lagging leg, the situation is more favorable because, at the time of the capacitance discharge, the primary side current is at its maximum and is mainly formed by the current flowing through the secondary filter inductance, which also participates in the capacitance discharge, defined by (3) [2, 13, 20]:

$$E_{L_{leading}} = 0.5Lk\left(I_{M,pk} + I_{L1,min}\frac{N_S}{N_P}\right)^2 \tag{2}$$

$$E_{L_{lagging}} = 0.5L_M I_{Mpk}^2 + 0.5L_1\left(\frac{N_P}{N_S}\right)^2\left(I_{L1,max}\frac{N_S}{N_P}\right)^2 + 0.5Lk\left(I_{Mpk} + I_{L1,max}\frac{N_S}{N_P}\right)^2 \tag{3}$$

where N_s is the number of secondary turns, N_p is the number of primary turns, I_{Mpk} is the peak of magnetizing current, I_{L1} is current in the output inductance and L_M is magnetizing inductance.

This indicates that achieving ZVS is easier for the lagging leg than for the leading one. Furthermore, (2) and (3) demonstrate that attaining ZVS depends on the current. One design approach is to add an auxiliary inductance that can provide enough inductive energy to discharge the capacitances in the no-load state at the leading leg. This means that only the magnetizing current of the transformer is enough to achieve ZVS. This solution will increase the efficiency in the no-load condition. The larger losses in the auxiliary inductance will cause an increase in losses at higher loads, limiting the current rise will limit the effective phase shift period, and the inductance will cause additional oscillations, so ultra-fast diodes are added to the circuit. Proper tuning of the circuit is, therefore, a question of application [2, 13, 20].

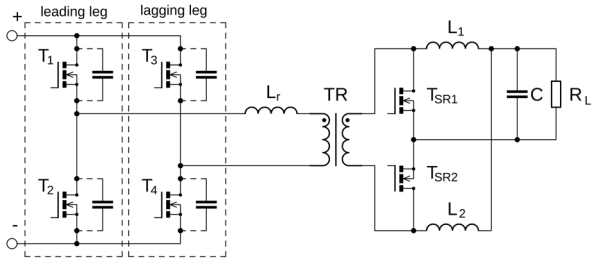

Figure 1
Schematic of PSFB converter with indicated legs

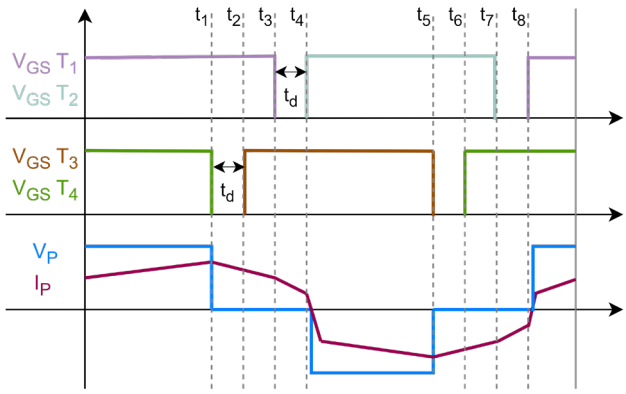

Figure 2
Switching diagram and primary voltage and current waveform

The second condition is to ensure sufficiently long dead time. The capacitive and inductive energy form a resonant circuit; thus, the voltage drops across the transistor in a resonant manner, Fig. 3. When the time is shorter than one-quarter of the resonant period $T_r/4$, the ZVS is lost [20]. If we lengthen the dead time, we will achieve ZVS, but there would be an unnecessary prolongation of the reverse diode conduction of the transistor, which will cause a further increase in losses [13] [20].

With a very long dead time, ZVS could be lost. Hence, the ideal dead time is exactly at the time when the voltage drops to zero. The problem is that inductive energy is different for both legs, so the dead-time is different and is still current dependent. The ideal would be to set the dead time differently for both legs and change it according to the load [14, 20, 21].

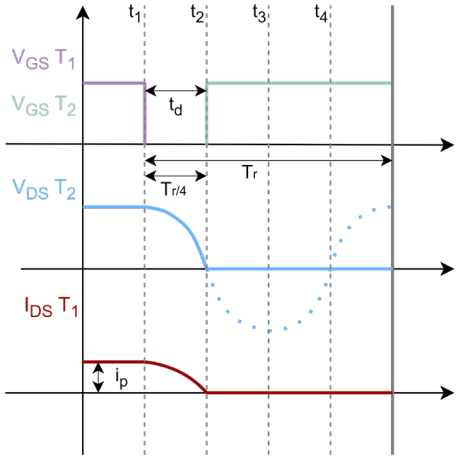

Figure 3
Collector voltage drop in a resonant way

The conclusion is that it is still beneficial to reduce the capacitance energy and, therefore, the output capacitance of transistors [2, 13, 15]. The waveform in Fig. 4 illustrates the voltage drop across transistors with different output capacitances ($C_{oss1} > C_{oss2}$) while the inductive energy remains unchanged together with the load. The figure illustrates that with a high output capacitance and the same inductive energy, ZVS may not be achieved even with a sufficiently long dead-time.

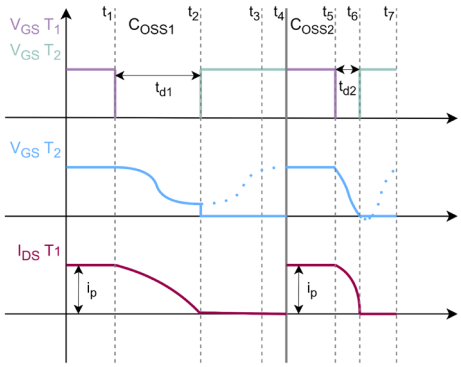

Figure 4
Illustration of the effect of different output capacitance ($C_{OSS1} > C_{OSS2}$) on the achievement of ZVS

3 Semiconductor Selection

Nowadays, the most used switching component for PSFB is the MOSFET transistor. Modern wide bandgap components based on SiC and GaN technology are slowly replacing the classic Si MOSFET transistors [15]. Table 1 compares three transistors of different technologies from Infineon for the same voltage and current levels.

As mentioned in the previous section, the goal is to achieve a low C_{oss} at a low R_{DSon}. This parameter is listed in Table 1 as a figure of merit R_{DSon}*C_{otr}. C_{otr} is C_{oss} but time-dependent, so it better describes the output capacitance in a resonant circuit. For high-frequency (HF) applications, it is good if the gate charge is low, as shown by the parameter R_{DSon}*Q_G.

Table 1

Infineon transistor technology comparison

	IPT65R190CFD7	IMT65R163M1H	GS-065-011
Technology	Si	SiC	GaN Hemt
V_{dsmax} (V)	650	650	650
I_d[1] (A)	16	19	11
R_{Dson} (Ω)	0.19	0.217	0.15
C_{otr}[2] (pF)	451	68	47
R_{Dson*} C_{otr} (Ω*pF)	85.69	14.76	**7.05**
Q_G (nC)	22	10	2.2
R_{Dson*} Q_G (Ω*pF)	4.18	2.17	**0.33**
Q_{rr} (nC)	440	39	**0**
t_{rr} (ns)	97	17	**0**

1- Continuous current at 25 °C

2- Time-related Coss, measure when the VDS was rising from 0 to 400V

Table 2

Transistor technology comparison

	IPDQ65R029CFD7	UF3C065030B3	LMG3426R030
Technology	Si	SiC	GaN Hemt
Manufacturer	Infineon	Qorvo	Texas Instruments
V_{dsmax} (V)	650	650	600
I_d[1] (A)	85	65	55
R_{Dson} (Ω)	0.029	0.027	0.03
C_{otr}[2] (pF)	2774	480	430
R_{Dson*} C_{otr} (Ω*pF)	80.45	**12.96**	**12.9**
Q_G (nC)	139	51	n.d[3]
R_{Dson*} Q_G (Ω*pF)	4.18	2.17	-

Q_{rr} (nC)	1600	211	**0**
t_{rr} (ns)	208	34	**0**

1- Continuous current at 25˚C
2- Time-related Coss, measure when the VDS was rising from 0 to 400V
3- GaN is integrated with a driver circuit

The Q_{rr} and t_{rr} parameters affect the reverse recovery losses. Table 2 shows a similar comparison of transistors from different manufacturers.

The above data shows that the best C_{otr} and R_{DSon} ratio is achieved with GaN technology, which is confirmed in both tables. It can also be observed that SiC technology is significantly better than Si, not only in the mentioned ratio but also in smaller reverse recovery losses. The advantage of GaN transistors is that they have no reverse recovery losses. A significant disadvantage of GaN transistors is that they are commonly available for voltage ranges up to 650 V, which, in combination with a single-phase PFC converter, as is the case here, is enough. However, for higher voltages up to 1200 V, SiC technology would be the better choice. For the proposed converter, the GaN transistors are the best option.

3.1 Converter Topology

The designed converter is shown in Fig. 1. The inverter is formed by transistors T_1-T_4, which switch with a duty cycle of 50% within the dead time. Output regulation is performed by changing the phase shift of the primary transistors.

Table 3
Parameters of the designed converter, transformer and output filter

Parameter	Value
Input voltage	390 V
Output voltage	24 V
Output power	600 W
Frequency	100 kHz
Transformer ratio	6
Filter inductance L_1 and L_2	30 μH
Filter capacitor C_O	56 μF

T_{SR1} and T_{SR2} form the synchronous rectifier, L_1, L_2 and C_O are the output filter and R is the load [16] [17]. The converter parameters were calculated with the help of [14] and are given in Table 3.

3.2 Simulation of GaN Transistors

Based on the previous chapter, GaN transistors from Infineon GaN Systems were chosen because they have better performance than Si and SiC for this type of application. The product line of transistors and their basic parameters are shown in Table 4. The transistors are from the 650 V series, and all have sufficient current capabilities for the proposed converter.

The components from Table 4 were simulated in the program Plecs, and their switching and conduction losses were simulated for a load range of 25% - 100%. These values are shown in Fig. 5. For a better visualization of the switching and conduction losses, the graphs in Fig. 6 - Fig. 9 have been created for each switching transistor.

Table 4
GaN System 650V product line

device	I_D[1] (A)	R_{DSon} (mΩ)	C_{otr}[2] (pF)
GS-065-030-2L	30	50	150
GS-065-018-1L	18	78	90
GS-065-011-1L	11	150	47
GS-065-008-1L	8	225	34
GS-065-004-1L	4	450	11

1- Continuous current at 25˚C
2- Time-related Coss, measure when the VDS was rising from 0 to 400V

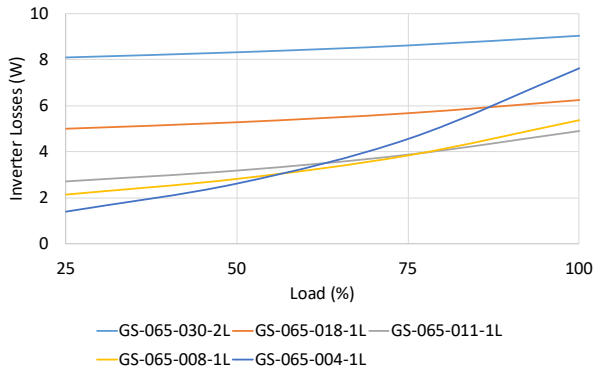

Figure 5
Losses of the inverter when changing the load

Based on the graphs, it is possible to see how the switching and conduction losses change within the operating range. For lower loads, a transistor with a small C_{oss} is preferred because a large amount of the losses are switching losses. At full load, a small R_{Dson} is advantageous due to the reduction of conduction losses.

The mentioned effect is also supported by the fact that achieving ZVS with a larger load current is easier.

The results of the simulations, as illustrated in Fig. 5, indicate that the most appropriate switching component for the proposed converter is GS-065-011.

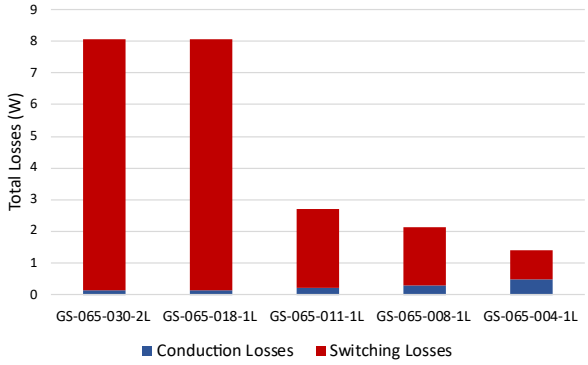

Figure 6
Inverter losses for each GaN transistor at 25% load

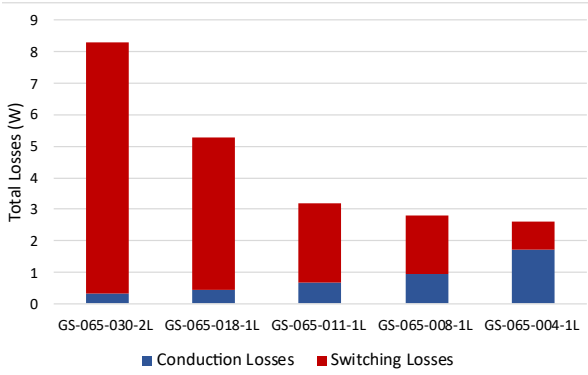

Figure 7
Inverter losses for each GaN transistor at 50% load

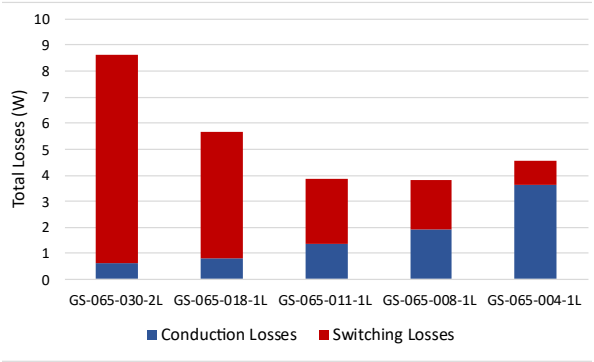

Figure 8
Inverter losses for each GaN transistor at 75% load

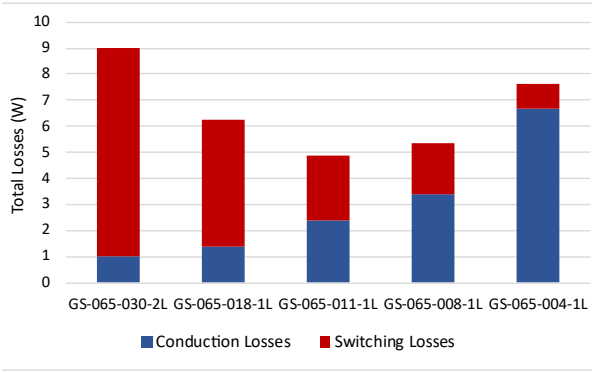

Figure 9
Inverter losses for each GaN transistor at 100% load

4 Laboratory Measurements

The inverter simulated in the previous chapter was measured under laboratory conditions with two types of GaN transistors on the primary side, **GS-065-018** and **GS-065-011**, respectively. A photo of the measurement is shown in Fig. 10.

The measurement was performed without additional inductance, only with the transformer leakage inductance, finding the load point where the inverter starts to reach ZVS. The leading leg of the inverter with **GS-065-018** transistors reached ZVS at 60% load, Fig. 11, and the lagging leg already at 29% load, Fig. 12.

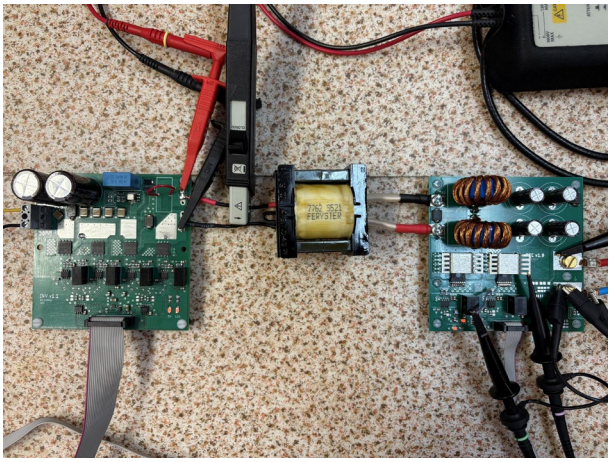

Figure 10
Laboratory measurements, left to right – inverter, transformer, rectifier

The **GS-065-011** transistors have a smaller output capacitance, so they achieve ZVS at a smaller load while maintaining the same inductive energy. The leading leg at 50%, Fig. 13, lagging leg at 11%, Fig. 14.

As was mentioned, achieving ZVS affects the efficiency of the inverter. It was confirmed in simulation that transistors with smaller output capacitance achieved lower losses at low load, but due to the larger R_{DSon}, conductive losses increased at higher load. For this reason, the efficiency of the whole converter was measured for both inverters, which is shown in Fig. 15.

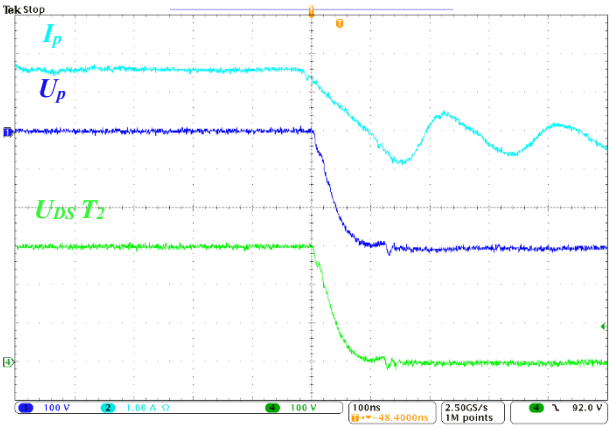

Figure 11
Leading leg ZVS, inverter with GS-065-018, load 60%

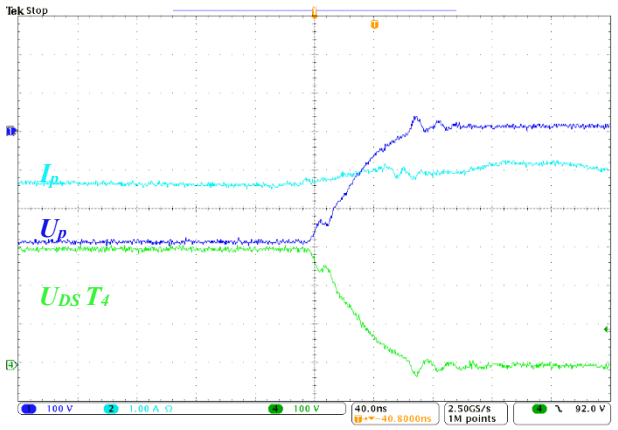

Figure 12
Lagging leg ZVS, inverter with GS-065-018, load 29%

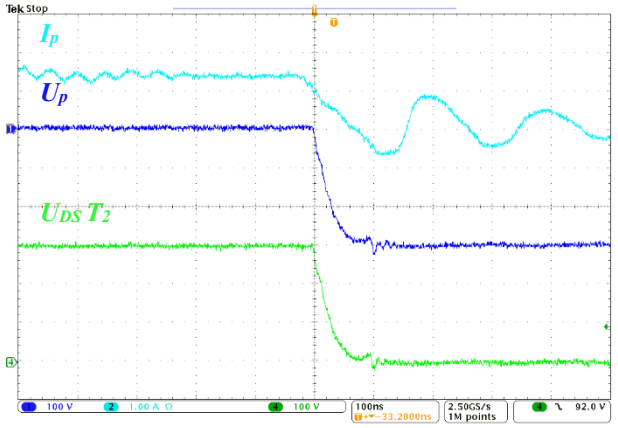

Figure 13
Leading leg ZVS, inverter with GS-065-011, load 50%

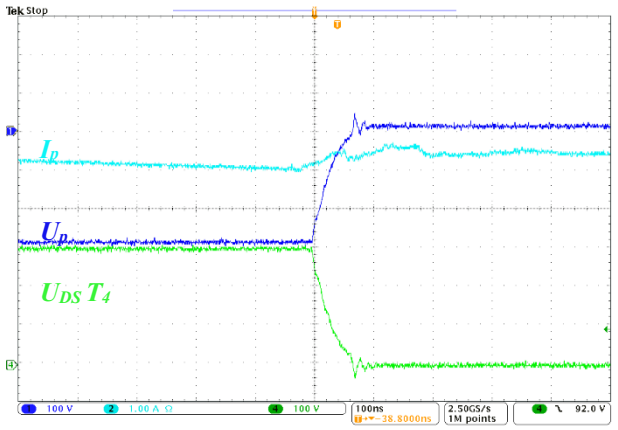

Figure 14
Lagging leg ZVS, inverter with GS-065-011, load 11%

In addition, thermal camera images were also taken for the inverter with GS-065-011, with a load of 50% in Fig. 16 and 100% in Fig. 17. For the inverter with GS-065-018, with a 50% load in Fig. 18 and a full load in Fig. 19. The temperature was measured after sufficient time in a quasi-steady state, when the temperature rise was negligible concerning time constant. This measurement is sufficient for comparing transistors with each other and declaring low losses indirectly. According to the schematic in Fig. 1, the transistors in the thermal camera images are shown from left to right, T_1 to T_4. Each transistor has a marked maximum temperature.

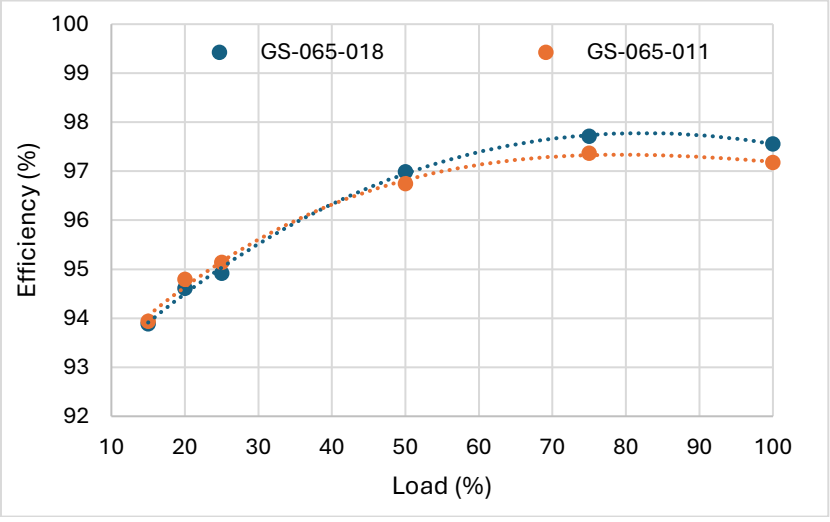

Figure 15
Comparison of PSFB converter efficiency for GS-065-011 and GS-065-018 GaN transistors in the inverter

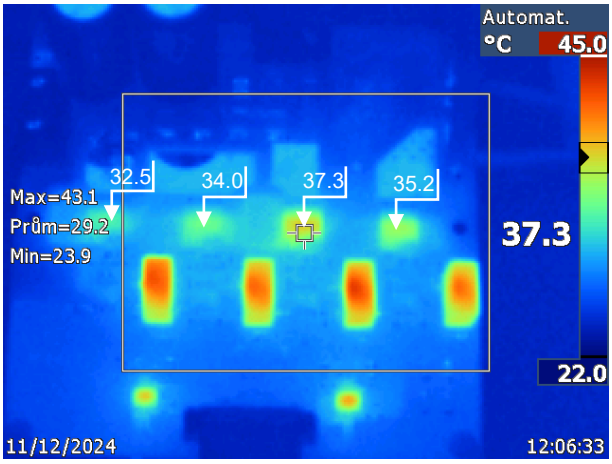

Figure 16
Thermal camera image, inverter with GS-065-011, 50% load

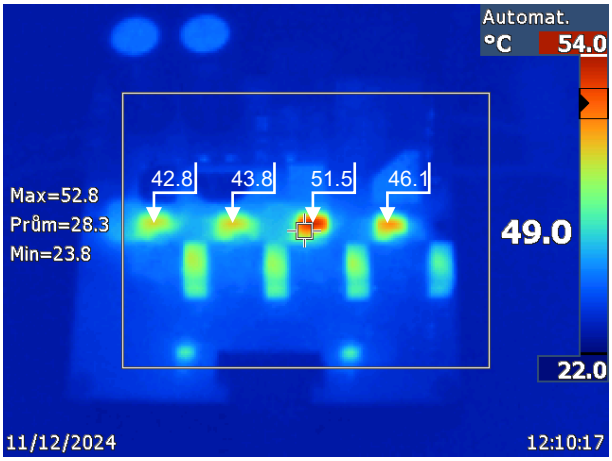

Figure 17
Thermal camera image, inverter with GS-065-011, 100% load

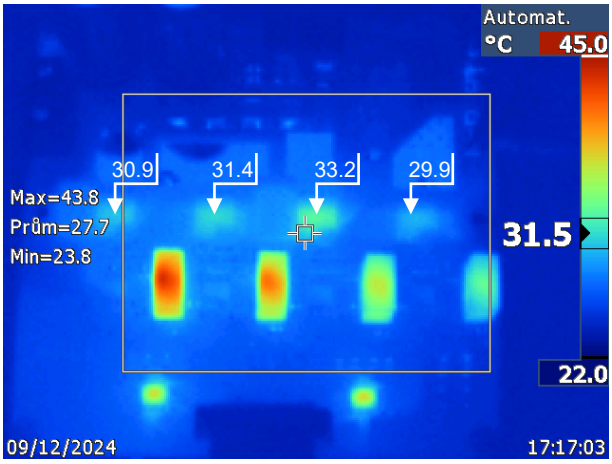

Figure 18
Thermal camera image, inverter with GS-065-018, 50% load

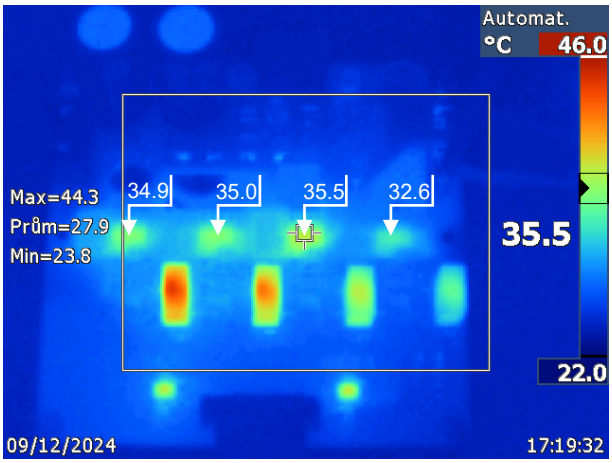

Figure 19
Thermal camera image, inverter with GS-065-018, 100% load

Conclusions

Transistor output capacitance plays an important role when designing a PFSB converter for a wide ZVS range. The converter holds different amounts of inductive energy, which is used for discharging the output capacitors. It is thus, beneficial to keep the output capacitances as low as possible. The simulation shows that the difference between GaN transistors ZVS range from the same family can be significant. However, the on-state resistance is also essential as it plays an important role in conduction losses for higher loads. The trade-off must be done, and the

detailed simulation can help to understand better the behavior of the PSFB converter in the whole load range. GaN transistors from Gan Systems were selected for simulation in Plecs, and the GS-065-011 transistor was selected as the best for the inverter with the lowest losses. Transistors with lower output capacitance had lower switching losses, which was particularly noticeable at light load, while transistors with lower resistance performed better at higher loads.

The results of measurements under laboratory conditions, in some ways, confirmed the simulation results and, in some ways, did not. The measurement confirmed that the inverter with the GS-065-011 transistor, which has a smaller output capacitance, achieved lower losses at lower loads and higher losses at higher loads compared to the inverter with the GS-065-018 transistor, which has a larger output capacitance. Still, according to the simulation, the GS-065-018 transistor should have had higher losses over the entire load range, which was also demonstrated by the image from the thermal camera, the GS-065-011 was reaching a higher temperature, already at 50% load. It should be noted that even the differences are not huge, they can have a significant influence on the cooling requirements or even on the decision to implement a passive heat-sink. Also, from a methodology point-of-view, the correlation between a power analyzer measurement and thermal imaging was completed.

Nevertheless, both inverters with GaN transistors were able to achieve ZVS without additional inductance, which made it possible to achieve high efficiency for a wide load range. This resulted in the elimination of additional magnetic component, thereby reducing the size and weight of the inverter. This is primarily due to the use of GaN transistors, which have an excellent ratio between series resistance and output capacitance, thereby enabling high efficiency to be achieved even when increasing the switching frequency.

Future research will include an evaluation of the influence of a variable dead time on the converter efficiency, as well as the increase in the power and switching frequency of the converter, also, the overvoltage oscillations limit the use of transistors with lower voltage ratings on the secondary side. This can increase the conduction losses of the converter, thus, it is crucial to apply the overvoltage protection in the form of an active snubber.

Acknowledgements

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